

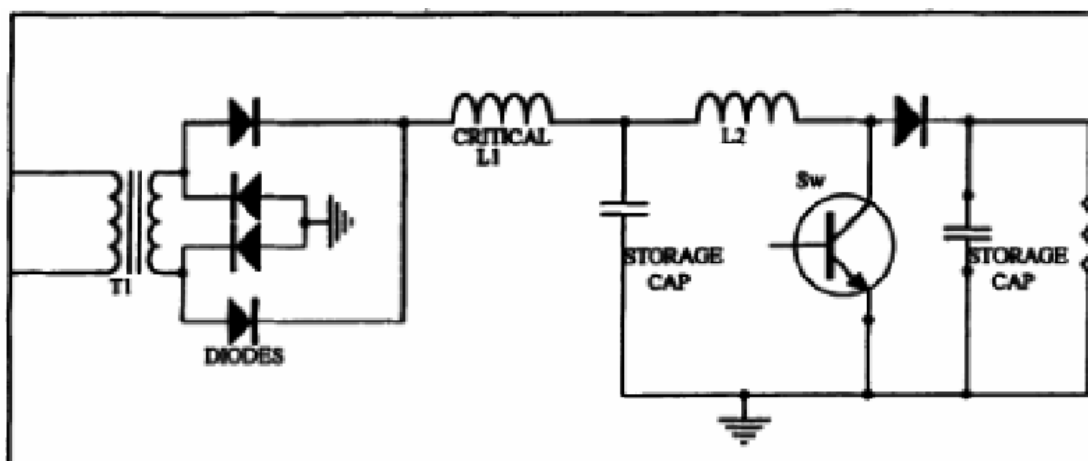


Figure 11.2 The off-line regulator with critical inductive and capacitive load.

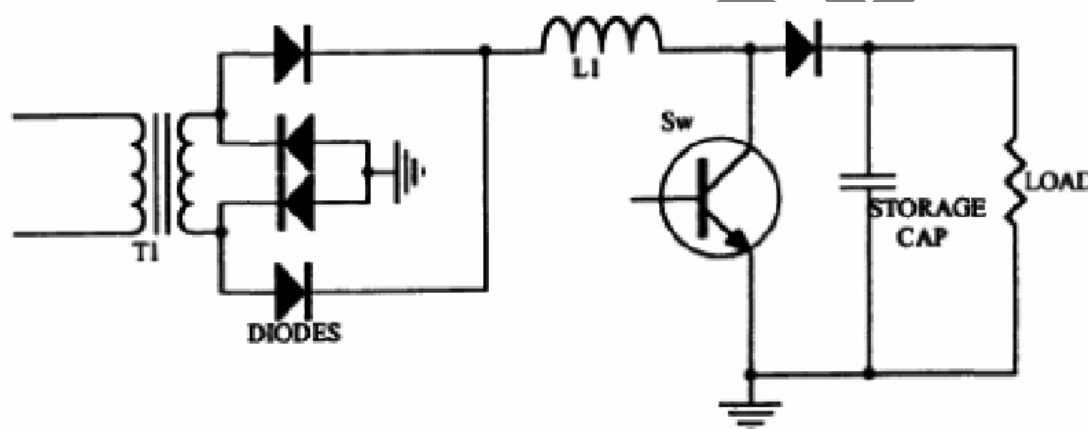


Figure 11.3 The power factor correction circuit.

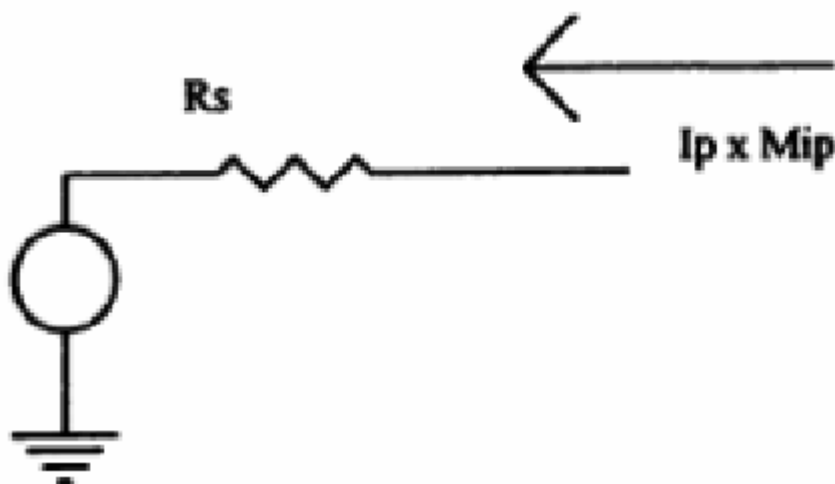


Figure 11.4 The line voltage source E_s , the source impedance R_s , and $I_p \times M_{ip}$.

The value of R_0 is the highest dc supply voltage divided by the lowest load current. The addition of the inductor lowers the storage voltage, but the power

supplied to the switcher(s) must be the same. This raise the current minimum, decreasing the value of R_0 and, therefore, L_c . This subject is covered by W.T. McLyman, *Transformer and Inductor Design Handbook* (Marcel Dekker).

R_0 是最高 DC 供电电压除以最低负载电流的值。这个附加的电感会降低储能电压，但对于向开关电源供电的电压则是相同的。这会使得电流增加很小并导致 R_0 和 L_c 值降低。这个问题在 Mclyman 的《变压器和电感设计手册 *Transformer and Inductor Design Handbook*》中有详细论述。

If the area product is known in centimeters to the fourth power, the approximate weight, in grams, and the volume, in cubic centimeters, can be estimated from Tables 11.1 and 11.2. These have been assembled from McLyman's book. The K_v factor multiplied by the A_p gives cubic centimeters, and K_w multiplied by A_p gives grams.

如果面积积已知，那么近似的重量（单位：g）和体积（单位：立方厘米）就可以由表 11.1 和 11.2 估算出来。这些数据表是从 Mclman 的书得来。 K_v 与 A_p 的乘积是立方厘米， K_w 与 A_p 乘积是克。

Laminations and tape-wound cores are rarely used for EMI filters but are included in Tables 11.1 and 11.2. Lamination information is needed for the critical inductance. The area product is the cross-sectional area of the core in square centimeters multiplied by the wire area or window area, also in square centimeters. The A_p must be multiplied by the stacking factor, if applicable (laminations and C cores). Continuing with McLyman's book, the value of the critical inductance must be found from Equation (11.1). The next step is to find the energy stored in the inductor.

EMI 滤波器很少使用迭片式和缠带式磁芯，但是相关的参数也列在表 11.1 和 11.2 中了。列出的有关迭片磁芯的信息是临界电感所需要的。面积积是磁芯横截面（单位：平方厘米）与绕线截面或绕线窗口面积的乘积。如要求 A_p 是可用的，那么需要乘以占空因数（对于迭片式和 C 型磁芯）。通过式 (11.1) 可以计算出临界电感值，下一步可以计算出电感储存的能量。

Table 11.1 Ratios of Area Product A_p to Weight and Volume

Core type	K_v (cm ³)	K_w (G)	x
Pot core	14.5	48.0	1.20
Powder core	13.1	58.8	1.14
Laminations	19.7	68.2	1.14
C core	17.9	66.6	1.16
Single coil	25.6	76.6	1.16
Tape wound	25.0	82.3	1.15

Table 11.2 Value of K_j for the Various Core Types

Core type	K_j (25°C)	K_j (50°C)	c
Pot core	433	632	1.20
Powder core	403	590	1.14
Laminations	366	534	1.14
C core	323	468	1.16
Single coil	395	569	1.16
Tape wound	250	365	1.15

$$ENG = \frac{L_c L_p^2}{2} \quad (11.2)$$

where I_p is the peak current the inductor must carry. The smallest load current determines the value of L_c , yet the peak of the largest charging current of the storage capacitor I_p through the inductor determines the energy that the inductor must handle. The minimum area product required to handle the energy is then, Per McLyman,

此处 I_p 为电感所必须承载的峰值电流。最小的负载电流决定 L_c 的值，通过电感的储能电容的最大充电电流的峰值可以确定电感承载能量的值。那么能承载此能量的最小面积积 (Mclyman 计算) 为：

$$A_p = \frac{[2(energy) \times 10^4]^X}{B_m K_w K_j} \quad (11.3)$$

here B_m is the maximum flux density, teslas, K_w is the winding factor for the type of core configuration chosen, and K_j (°C), comes from Table 11.2 (from McLyman's core configuration table above).

此处 B_m 为最大磁通密度，单位为特斯拉， K_w 为选定的磁芯类型的绕线因数， K_j (°C) 来自于表 11.2。

The design should be for 25°C to reduce the temperature rise of the entire filter. This may be a good recommendation for the critical inductor, too, but the savings in volume and weight would be greater with a 50°C temperature rise for the critical inductor if the surrounding circuits can withstand it. X is repeated here for convenience.

为减小整个滤波器的温升，设计中需要选择 25°C 条件下参数。对于临界值电感此参数也同样是一个较好的建议值，但是如果临界电感周围的电路能耐受 50°C 的温升，那么使用 50°C 条件的参数会大大减小此电感的体积和重量。为方便，此处重复列出了 X 值。

If the pulse current charging the storage capacitor, without the critical inductor, is integrated, from Section 3.2, the approximate area under the curve (pulses) can be calculated:

在没有临界值电感的情况下，对储能电容的充电电流脉冲进行积分，使用 3.2 节的表达式，得到脉冲曲线下近似的面积为：

$$\frac{2t}{pT} + \frac{4tT}{p} \sum_{N=2,4,6,8}^{\infty} \frac{1}{T^2 - N^2 t^2} \cos \frac{pNt}{2T} \cos \frac{pN}{2} \cos \frac{2pNt}{T} \quad (11.4)$$

or

$$\frac{2t}{pT} + \frac{4tT}{p} \sum_{N=2,4,6,8}^{\infty} \frac{(-1)^{N/2}}{T^2 - N^2 t^2} \cos \frac{pNt}{2T} \cos \frac{2pNt}{T} \quad (11.5)$$

$$\int_0^{T/2} \frac{2t}{pT} dt + \int_0^{T/2} \frac{4tT}{p} \sum_{N=2,4,6,8}^{\infty} \frac{(-1)^{N/2}}{T^2 - N^2 t^2} \cos \frac{pNt}{2T} \cos \frac{2pNt}{T} dt \quad (11.6)$$

$$\frac{2t}{pT} t \Big|_0^{T/2} + \frac{T}{2p} \frac{4tT}{p} \sum_{N=2,4,6,8}^{\infty} \frac{(-1)^{N/2}}{N(T^2 - N^2 t^2)} \cos \frac{pNt}{2T} \sin \frac{2pNt}{T} \Big|_0^{T/2} \quad (11.7)$$

$$\frac{T}{p} + \frac{2tT^2}{p^2} \sum_{N=1,2,3,4}^{\infty} \frac{(-1)^{N/2}}{N(T^2 - N^2 t^2)} \cos \frac{pNt}{2T} \sin pN \quad (11.8)$$

where the summation must change after integration. The sine of any integer multiplied by π is zero

此处积分后总和发生了变化。 π 的整数倍弧度的正弦值为零。

$$\sin pN = 0 \quad (11.9)$$

and thus the area under the curve reduces to

此时曲线下的面积减小为

$$\frac{t}{p} \quad (11.10)$$

As the value of the storage capacitor increases, τ is reduced, reducing the width under the curve, but the peak increases, making the area the same. The area here is normalized to 1, so the peak is the reciprocal of Equation (11.10):

当储能电容增加, τ 会减少, 此时曲线宽度减小但峰值增加, 结果是面积不变。此处的面积值归一化为 1, 所以式 (11.10) 的倒数为

$$\frac{p}{t} \quad (11.11)$$

If the conducting angel is 20° , τ is

如果传导角为 20° , 那么 τ 为:

$$t = \frac{p}{9} \quad (11.12)$$

and the peak current is

峰值电流为

$$\frac{p}{p} = 9$$

This is normalized for a current of 1 A, so the multiplier is 9; 4 A would give a peak of 36 A for the 20°. In degrees, the peak multiplier is

电流归一化为 1A, 所以乘数为 9: 4A 在 20° 传导角下为 36A。以度为单位, 峰值乘数为

$$\frac{180}{\text{conduction angle, degrees}} \quad (11.13)$$

This agrees with the calculations of Mike Hannigan at Powerlab (Pomona, CA 91798).

这个角度公式是由电源实验室的工程师 Mike Hannigan 推导出来的。

What is lacking is the conduction angle in either degrees or radians. This is developed next. From Equation (3.7), the peak-to-peak ripple varies with the capacitor value and is repeated here:

目前缺少的是传导角可以用度和弧度表示的表达式。下面将会推导这一公式。从等式 (3.7) 可得峰-峰值纹波随电容值变化表达式, 此处再次写出:

$$C = \frac{I_0 10^6}{2F(P - P)} \text{ mF} \quad (11.14)$$

where I_0 is the load current. The peak to peak (P-P) ripple as a function of C, farads, and F, the line frequency, and I_0 is as follows:

此处 I_0 是负载电流。峰-峰值纹波是电容 C (法拉第) 的函数, F 为电源线频率, I_0 值如下:

$$P - P = \frac{I_0}{2FC} \quad (11.15)$$

The capacitor charges to V_p : less line, wire, transformer (if any); and diode loss. All losses are ignored. The minimum capacitor voltage, V_0 is as follows:

电容器充电到电压 V_p : 减去电源线、导线、变压器 (如果有的话) 和二极管的损耗。即忽略所有损耗, 最小电容电压 V_0 如下:

$$V_0 = V_p - (P - P) = V_p - \frac{I_0}{2FC} = \frac{2V_p FC - I_0}{2FC} \quad (11.16)$$

The ratio V_0/V_p is as follows:

V_0/V_p 的比值如下:

$$\frac{V_0}{V_p} = \frac{2V_p FC - I_0}{2V_p FC} \quad (11.17)$$

Knowing this ratio in Equation (11.17) and the ratio:

如果已知式 (11.17) 中的比值和下面的比值：

$$\frac{1}{\omega R_0 C} = \frac{1}{2pFR_0 C} \quad (11.18)$$

the current conduction angle (radians) through the diodes can be calculated.

This is the conduction angle of each pulse:

那么电流流过二极管的传导角（弧度）就可以计算出来了。对于每个脉冲其传导角为：

$$t = \cos^{-1} \frac{V_0}{V_p} + \sin^{-1} \frac{1}{2pFR_0 C} \quad (11.19)$$

and the current peak multiplier follows:

且峰值电流乘数为：

$$M_{ip} = \frac{p}{t} = \frac{p}{\cos^{-1} V_0 / V_p + \sin^{-1} 1 / 2pFR_0 C} \quad (11.20)$$

R_0 is selected as a minimum to give the smallest peak current for the minimum size of inductor in the EMI filter. This is when

尽量选择最小的 R_0 以得到最小的峰值电流。这样 EMI 滤波器中电感尺寸就最小。

$$R_0 = \frac{V_0}{I_0} = \frac{2V_p FC - I_0}{2FCI_0} \quad (11.21)$$

and

$$M_{ip} = \frac{p}{\cos^{-1} V_0 / V_p + \sin^{-1} I_0 / 2pFV_0 C} \quad (11.22a)$$

or

$$M_{ip} = \frac{p}{\cos^{-1} \left[(2V_p FC - I_0) / 2V_p FC \right] + \sin^{-1} \left[I_0 / p (2V_p FC - I_0) \right]} \quad (11.22b)$$

showing that M_{ip} depends on V_p , the peak voltage, F , the line frequency, I_0 , the dc load current, amperes, and C , farads. Now that M_{ip} is known, the energy can be found for the inductors in the EMI filter. The denominator of these equations must be in radians.

可以看到 M_{ip} 的大小依赖于峰值电压 V_p 、电源线频率 F 、DC 负载电流 I_0 和 C （单位：法拉第）。现在知道了 M_{ip} 的值后就可以计算出 EMI 滤波器中电感所储存的能量。这些表达式中的分母使用的是弧度的单位。

There is no way to calculate the needed loss of the filter from this information.

Assume a double-balanced L with each inductor, four, at 250 uH each. This size of inductance is purposely made small for this amount of current to prove further that if this size meets the requirements, larger inductances surely will. Also, assume a 60 Hz line with a V_p , of 167 V capacitor of 2000 uF, and a load current of 5 A. Then M_{ip} is 5.7096, or 5.71. This means that the peak current is 5 multiplied by the 5.71 multiplier, or 28.55 A.

通过以上这些信息还不能计算出需要的滤波器插损值。假设一个平衡双 L 型电路，4 个电感每个值均为 250uH。在此负载电流下，这些电感的尺寸故意取较小的值，因为如果此尺寸能满足要求，那么更大的电感就更能满足要求了。同样，假设电源线频率为 60Hz、峰值电压为 167V、电容值为 2000uF、负载电流为 5A，那么 M_{ip} 为 5.7096 或近似为 5.71。这就意味着峰值电流为 5 乘 5.71 结果为 28.55A。

$$ENG = \frac{250 \times 10^6 \times 28.55^2}{2} = 0.1019 \quad (11.23)$$

From this, the A_p for the EMI inductor follows. Choosing the powder core toroid with a winding factor K_M of 0.4 and a B_m of 0.7 T, the MPP maximum flux density, the values of K_j (at 25°C), K_v , K_w , and X are taken from Table 11.2:

通过此值，得到 EMI 电感的 A_p 值如下。选择绕线常数为 0.4 和最大磁通密度为 0.7T 的粉芯圆环中的 MPP 环，其中 K_j (at 25°C)、 K_v 和 K_w 的值取自表 11.2：

$$K_j = 403 \quad X = 1.14 \quad K_v = 13.1 \quad K_w = 58.8$$

$$A_p = \frac{[2(energy)10^4]^X}{B_m K_M K_j} \quad (11.24)$$

$$A_p = \frac{(2 \times 0.1019 \times 10^4)^{1.14}}{0.7 \times 0.4 \times 403} = 52.484 \quad (11.25)$$

For each inductor, or multiplied by 4,
对于每个电感，乘以 4，

$$\frac{4 \times 52.484 \times 13.1}{2.54^3} = 167.825 \quad (11.26)$$

or 168 inches³, or approximately $10 \times 4.25 \times 4.25$, and the weight is 27.2 pounds, per

近似为 168 立方英寸，或近似为 $10 \times 4.25 \times 4.25$ ，对于重量通过下式得到，其值为 27.2 磅。

$$\frac{4 \times 52.484 \times 58.8}{453.6} = 27.214 \quad (11.27)$$

Large and heavy? Yes! Most designers do not allow for this amount of peak current, and so their filters are smaller and lighter but often saturate on the peak of the current pulse. Worse yet is that these are current pulses at twice the

line frequency-for a single phase-and the pulse permeability is low than normal, further reducing the inductance value.

这个电感又大又重？当然！多数设计者并不会考虑此峰值电流，所以他们设计的滤波器会体积很小并很轻。但是在脉冲的峰值电流条件下，磁芯常常饱和。较差的情况是，对于单相条件下两倍于电源线频率的电流脉冲会导致磁导率低于正常的值，这会降低电感的值。

With the critical inductance, the 167 V_{peak} is reduced to average, or
安装临界电感后，167V 的峰值电压降低到平均值，或

$$167 \times 0.637 = 106.379 \quad (11.28)$$

The power must be the same, or the current is of the order of 7.87 A. The minimum current for sizing the inductor is 0.5 times the current, or 4 A. This makes the value of R_0 equal to 26.5Ω . The critical inductor value is as follows:
其功率必定与之相同，或电流为 7.87 的规定值，决定电感尺寸的最小电流就是此电流的 0.5 倍即 4A。这样 R_0 的值就等于 26.5Ω ，而电感临界值如下：

$$L_c = \frac{R_0}{6pF} = \frac{26.5}{6 \times p \times 60} = 0.023H \quad (11.29)$$

and the energy is

且能量为

$$\frac{0.023 \times (7.87)^2}{2} = 0.712$$

The area product is as follows:

面积积如下：

$$A_p = \frac{[2(energy)10^4]^X}{B_m K_w K_j} \quad (11.30)$$

where K_w is 0.6, K_j is 534, K_v is 19.7, K_w is 68.2, B_m is 1.8 T, and X is 1.14 for laminations given in Table 11.2.

此处 K_w 为 0.6、 K_j 为 534、 K_v 为 19.7、 K_w 为 68.2、 B_m 为 1.8 T，且对于叠片结构表 11.2 给出 X 为 1.14。

$$A_p = \frac{(2 \times 0.712 \times 10^4)^{1.14}}{1.8 \times 0.6 \times 534} = 94.197 \quad (11.31)$$

From the area product for the critical inductor, volume is calculated in cubic inches:

通过临界电感的面积积，可以计算出以立方英寸为单位的体积如下：

$$\frac{94.2 \times 19.7}{2.54^3} = 113.244 \quad (11.32)$$

and the weight in pounds is

和以磅为单位的重量为：

$$\frac{94.2 \times 68.2}{453.6} = 14.163 \quad (11.33)$$

The question is, will the filter inductors, four again, fit within the remainder of volume and weight?

现在问题是，此 4 个滤波器电感是否能符合剩余的体积和重量的要求？

The peak current is

峰值电流为

$$7.78\sqrt{2} = 11.003 \quad (11.34)$$

The filter inductor energy is

滤波器电感储存的能量为

$$\frac{0.00025 \times (11)^2}{2} = 0.015 \quad (11.35)$$

and the area product is

且乘积积为

$$A_p = \frac{(2 \times 0.015 \times 10^4)^{1.14}}{0.7 \times 0.4 \times 403} = 5.903 \quad (11.36)$$

The volume is, in cubic inches,

以立方英寸为单位的体积为

$$\frac{4 \times 5.908 \times 13.1}{2.54^3} = 18.892 \quad (11.37)$$

and the weight in pounds is

以磅为单位的重量为

$$\frac{4 \times 5.908 \times 58.8}{453.6} = 3.063 \quad (11.38)$$

The total weight, in pounds, of the critical inductor and filter inductors is

滤波器电感和临界电感的总重量为（单位：磅）

$$14.163 + 3.063 = 17.227 \quad (11.39)$$

which is well below the 27.2 pounds of the filter without the critical inductor. The

total volume, in cubic inches, of the critical inductor and the filter inductors is

这个重量远轻于没有临界电感的滤波器重量。滤波器电感和临界电感的总体积为（单位：立方英寸）

$$113.244 + 18.892 = 132.136 \quad (11.40)$$

This is again less than the filter alone without the critical inductor, which was

168 inches³. The filter capacitors were not included because they would be almost the same volume and weight with or without the critical inductor. There is a further savings in volume and weight in the storage capacitor. The capacitive reactance value of the storage capacitor with L_c should be equal to, or less than, $1/10R_0$ at the ripple frequency, 120 Hz in this example (twice the 60 Hz). This is, per McLyman, Powerlab, and others,

这个体积值也远小于没有临界电感的 168 立方英寸体积的情况。因为有和无临界电感时电容的体积和重量几乎相同，所以此计算没有包括滤波器电容。这更进一步节省了储能电容的重量和体积。储能电容的容抗和 L_c 在纹波频率下应小于等于 $1/10 R_0$ 。此例中为 120Hz (两倍于 60Hz)。这是由 Mclyman 和其它人导出的。

$$\frac{R_0}{10} = \frac{26.5}{10} = 2.65^\circ C = \frac{1}{2p \times 120 \times 2.65} = 500mF$$

The storage capacitor would be about a quarter of the size using the critical inductor in this example. This further reduces the weight and volume.

在使用临界电感的这个例子中，储能电容大约为此尺寸的 1/4。这进一步降低了重量和体积。

Another advantage of employing the critical inductor is that, with its dc and inductive reactance, it aids the reduction of the in-rush current. This example used quite small EMI filter inductors, and if these are calculated as around 400 uH, the illustrated example would have been much more severe.

使用临界电感的另一个优点是，临界电感的 DC 电阻和感抗会降低涌入电流。本例使用了一个非常小的 EMI 滤波器电感，但如果使用一个约 400uH 的电感时，这种减小体积和重量的情况会更剧烈。

§11.2 The Added Power Line Harmonic Content Caused by the Off-Line Regulator

§11.2 由离线调节器产生的额外的谐波量

From Equations (11.22) and (3.2), the increase in the harmonic current content of the power line can be discussed.

通过 (11.22) 和 (3.2)，我们可以讨论一下电源线谐波电流增加的情况。

$$M_{ip} = \frac{p}{\cos^{-1}[(2V_p FC - I_0)/2V_p FC] + \sin^{-1}[I_0/p(2V_p FC - I_0)]} \quad (11.41)$$

In the first equation, the denominator is τ in radians. In the next equation τ is in seconds.

第一个等式中，分母中 τ 的单位是弧度。而在第二个等式中 τ 的单位是秒。

$$I_{(t)} = \frac{4tT}{p} \sum_{N=1,3,5,7}^{\infty} \frac{1}{T^2 - N^2 t^2} \cos \frac{pNt}{2T} \sin \frac{pN}{2} \sin \frac{2pNt}{T} \quad (11.42)$$

The two terms π and τ , one in each equation, do not cancel. The best technique

is to solve for M_{ip} and then multiply $I_{(t)}$ by M_{ip} . The π terms can cancel, but one of the τ terms must be changed for clarity. One method is to compare the ration of τ and T to 2π to convert the time τ in seconds to radians. This gives the approximate equation of the current created by the off-line regulators. This would still be very approximate, because V_p in the first equation would decrease as the pulse current charging the capacitors increases. This, in turn, would increase the value of τ , the conduction angel (degrees or radians). In the second equation, the first sine term for $N=\text{odd}$ is

每个等式中的 π 和 τ 项并没有被消掉。最好求解 M_{ip} 的方法是先求出 M_{ip} ，然后将 $I_{(t)}$ 乘以 M_{ip} 。 π 项可以消去，但是对于 τ 项为使表达式更清楚，需要进行转换。可以通过对比 τ 和 $T/2\pi$ 来实现时间 τ 到弧度的转换。这样就给出了离线调节器产生的电流的近似表达式。这种近似是误差很大的，这是因为第一个等式中的 V_p 在脉冲电流对电容充电时会降低。这会增加 τ 的值和传导角（度或弧度）。在第二个等式中，对于第一个正弦项 $N=\text{奇数}$ 时为

$$\sin \frac{pN}{2} = (-1)^{(N-1)/2}$$

or

$$\frac{2t}{pT} + \frac{4tT}{p} \sum_{N=2,4,6,8}^{\infty} \frac{(-1)^{(N-1)/2}}{T^2 - N^2 t^2} \cos \frac{pNt}{2T} \sin \frac{2pNt}{T}$$

The EMI filter is purposely not shown or is a typical commercial filter that provides little loss at these low frequencies of interest. These current peaks from the off-line regulators distort the sine wave source voltage E_s . This is a result of the voltage drop in the line impedance R_s for all loads fed by this source. If the conduction angle is 20° , as before, the value of M_{ip} is 9.

此处故意没有安装 EMI 滤波器，或是只安装了一个在低频几乎没有损耗的商用滤波器。这样这些离线调节器产生的电流峰值就会影响正弦波源电压 E_s 。对于所有负载来讲，这是电源在线路阻抗 R_s 上产生压降的结果。如果传导角为 20° ，那么如前述， M_{ip} 值为 9。

If Power factor correction circuits, inductive input power supplies, and better EMI filters are employed, $I_p \times M_{ip}$ is greatly reduced and approaches RMS.

如果采用功率校正因数、电源感性输入端口并选用较适合的滤波器，那么 $I_p \times M_{ip}$ 的值就会极大地降低，并接近平均值。

Hundreds of these off-line regulators can be fed by this source, and these current pulses create some degree of flatness in the voltage sine wave. At remote sites where the generator can just handle the required load, actual drains occur at the peak of the voltage sine wave.

这个电源可能为几百个离线调节器提供馈电，此时这些电流脉冲就会在正弦电压波上生成一些畸变。在能够满足负载需求的发电机所在的远端，实际的波形衰落发生在正弦电压波的峰值处。

If the filter designer is not also the power supply designer, or at least part of the group, try to find out whether power factor correction or an inductive input is employed. Attempt to have the design group use either of these if they want a smaller and less expensive EMI filter for their supply.

如果滤波器设计者不是电源设计者，那滤波器设计者就需要了解电源是否使用了功率因数校正电路或感性输入电路。如果想要在电源上使用小体积和低成本的 EMI 滤波器，就需要在电源上使用这两种电路中的一种。

If the system will be used in areas of quality power and either of the techniques of ridding the supply of high current pulses is used, there should be little worry about the harmonic currents or specifications for the capacitors making up the EMI filter. If these conditions are unknown, stick with foil capacitors that support higher pulse currents.

如果系统使用了高品质的电源，而且使用了消除电源大电流脉冲的二个电路中的一个，那么就不需要顾及谐波电流或制作 EMI 滤波器的电容要求了。如果这些假设是未知的，那么就要坚持使用能承载高脉冲电流的金属箔电容。

EMCARE

12

Initial Filter Design Requirements

初始的滤波器设计需求

The goals of this chapter are as follows:

1. Differential mode design goals
2. Common mode design goals
3. Estimate of common mode load impedance

This chapter discusses these goals and what can happen if they are not met.

本章的目标如下：

1. 差模设计
2. 共模设计
3. 估算共模负载阻抗

这一章将讨论这些问题，并讨论如果不满足这些目标时会发生什么情况。

§12.1 Differential Mode Design Goals

§12.1 差模设计

§12.1.1 Input Impedance of the Filter

§12.1.1 滤波器输入阻抗

The idea is to make the filter transparent to the line. This is ideal for both ac and dc systems and really means that the load impedance is transferred to the input of the filter at the line frequency, along with most of its harmonics. The harmonic content depends on the quality of the line. The poorer the line, the more distorted the sine wave shape becomes. These harmonics are odd harmonics. The filter cutoff frequency to accomplish this goal should be above the ninth harmonic. This is because the level of any harmonic above the ninth, even for the poorest quality line, is insignificant. This is why the rule is set at the tenth harmonic of the line frequency.

滤波器输入阻抗设计的思想是使滤波器对电源线透明。对 AC 和 DC 系统，这一思想意味着负载阻抗在电源线频率和多数谐波频率下可以传递为滤波器的输入阻抗。通常谐波量与电源线质量有关，电源线越差，正弦波就畸变得越厉害。因为这些谐波是奇次谐波，所有为达到以上的目标就要求滤波器的截止频率高于 9 次谐波，这是因为在高于 9 次得谐波的情况下，即使是质量最差的电源线也是无关紧要得。这也是将截止频率设为 10 次谐波的原因。

$$Z_{if} \text{ at } N_{fi} = R_i \quad (12.1)$$

where Z_{if} is the input impedance of the filter, N is the harmonic number and is set equal to 10, and R_i is the load impedance at the same frequency. Practically speaking, the load impedance is constant over the frequency range of interest

in this discussion.

此处 Z_{if} 是滤波器输入阻抗， N 为谐波级数并设为 10， R_l 是同样频率下的负载阻抗。实际上，在我们讨论中所感兴趣的频段下，负载阻抗为常数。

This goal is hard to reach, especially for high-current filters in which the required losses are heavy at the low-frequency end. The filter designer should strive to reach this goal, however. If the cutoff frequency allows the filter to attenuate the fifth harmonic and some of the third harmonic, higher capacitor currents result. These heat the capacitors because of the current through the ESR. The higher harmonic currents through the inductors also heat the capacitors because of the current through the dc resistance and higher core losses. This raises the operating temperature of the filter. The low cutoff frequency lowers the resonant rise frequency and raises the circuit Q . Either of these increases the odds that the filter will oscillate.

上面的这个设计目标非常难达到，尤其是在低频端对损耗要求较高的大电流滤波器，当然滤波器设计者应努力达到这一目标。如果截止频率取值允许滤波器衰减 5 次谐波和部分 3 次谐波，那么流过电容器的电流就很大。此时由于电流流过电容器 ESR 的缘故，会使得电容温度升高。另外，通过电感的谐波也会加热电容器，这是因为电感的 DC 阻抗和磁芯损耗会产生热量。这些都会升高滤波器的工作温度。低的截止频率降低了谐振增益频率并提高了电路的 Q 值，这两个因素都会增加滤波器振荡的几率。

§12.1.2 Output Impedance of the Filter

§12.1.2 滤波器输出阻抗

This section follows the same logic as for the input impedance of the filter. The filter should be transparent to the load. If the input impedance goal is met, the output impedance goal is also normally met. Meeting these two goals makes for better filter operation.

本节遵循的理论是与滤波器输入阻抗相同的：滤波器应对负载透明。其实如果满足了输入阻抗的目标，那么输出阻抗的目标也同样会得到满足。当然满足这两个目标，会使滤波器工作良好。

$$Z_{of} \text{ at } N_{fi} = R_l \quad (12.2)$$

where Z_{of} is the filter output impedance and R_l is the line impedance at the same frequency. The other terms are the same. The line impedance here is the basic dc resistance of the line. This is true for most lines to 5 kHz before any rapid increase to higher line impedances is reached. At 10 kHz the impedance is about 4 Ω on most lines.

此处 Z_{of} 是滤波器输出阻抗， R_l 是相同频率下的电源线阻抗。此处的电源线阻抗是线的 DC 阻抗，在 5kHz 前（在电源线阻抗快速增加到高线阻抗前）多数线缆都是如此。但在 10kHz 情况就不同了，此时多数线缆阻抗约为 4 Ω 。

§12.1.3 Input and Output Impedance for a DC Filter

§12.1.3 DC 滤波器的输入和输出阻抗

Both of the two preceding requirements are easily met for a dc system unless

the load is a switcher. Here, the output impedance of the filter must be very low. This statement rests on the premise that the switcher designer has not anticipated this.

对于 DC 系统，除了负载是开关电源的情况，前面所提到的两个要求都会很容易得到满足。此处滤波器的输出阻抗必定十分低，正如前面所说的，实际上开关电源设计者并没有预见到这一点。

$$Z_{of} \text{ at } F_{sw} \ll R_l \text{ at } F_{sw} \quad (12.3)$$

where F_{sw} is the switch frequency and the rest of the terms are the same. The same holds true at the tenth harmonic of the switcher frequency. The switch may not be all that starved at the fundamental and yet be starved at the ninth or eleventh harmonic, if the output impedance is slightly inductive or the output capacitor is above its self-resonant frequency. Little power is carried by the higher frequencies above the ninth harmonic, so these may be attenuated.

此处 F_{sw} 是开关频率。在开关频率的 10 倍谐波频率下此式同样是正确的。如果输出阻抗呈轻微的感性或输出电容工作在 SRF 之上，那么开关电源波形就不完整：在基波和 9 或 11 次谐波都会产生“饥饿”现象。由于高于 9 次的高频谐波只携带很少的能量，因此这些能量可以被衰减。

If this goal is not met, the switch is starved. The output impedance of the filter should be of the order of 0.1 of the load impedance during conduction or on time. This is also a function of the pulse width. The main goal is to ensure that the drop is not excessive so that the switcher can function properly. For example, $F_{sw}=80 \text{ kHz}$, $V_s=28 \text{ V}$, $I_{on}=8 \text{ A}$ during on time, and $t=5 \text{ us}$ =pulse width.

如果不能满足式 (12.3)，那么开关电源就会产生“饥饿”现象。通常在工作时滤波器的输出阻抗应为负载阻抗的 0.1 倍的量级，同时它也是脉冲宽度的函数。这样做主要的目的是要保证电压不会降低过多，使得开关电源能正常工作。例如，工作时 $F_{sw}=80 \text{ kHz}$, $V_s=28 \text{ V}$, $I_{on}=8 \text{ A}$ ，脉冲宽度 $t=5 \text{ us}$ 。

The on impedance followed by the required capacitor impedance and then followed by the capacitor value is

通路阻抗、所需的电容阻抗和电容值如下

$$\frac{28}{8} = 3.5 \quad \frac{3.5}{10} = 0.35 \quad C = \frac{1}{2\pi 80,000 \times 0.35} = 5.68 \text{ mF} \quad (12.4)$$

The output impedance of the filter at 80 kHz to meet the requirement is, from Equation (12.1), 0.35, and the capacitor value is 5.68 uF. Use a close value.

通过式(12.1)得到，符合要求的滤波器在 80kHz 的输出阻抗为 0.35，且电容值为 5.68uF。电容可以使用接近的值。

This goal requires a very good quality capacitor with a self-resonant frequency above at least the fifth harmonic of the switcher frequency, 400 kHz in this example. The value of the capacitor can be rounded to the closest standard value.

为满足上面的要求，此时就需要一个 SRF 至少在开关频率的 15 次谐波频率之上的高品质电容，此例是 400kHz。电容值可以近似取值到最邻近的标准电容值。

§12.2 Common Mode Design Goals

§12.2 共模设计

The common mode need not meet any of these requirements for the differential mode. The cutoff frequency can be as low as desired, cutting well into power harmonic frequencies. Watch for leakage inductance in Zorro inductor(s). This generates a high amount of differential mode inductance and can saturate the inductors at the current peaks.

共模设计并不需要满足差模设计的那些需求。共模设计的截止频率选多低都可以，可以低到截止频率切入到谐波频率中也没有问题。但需要注意 Zorro 电感的漏感，这些漏感产生了较大的差模电感，并会在电流峰值处导致电感饱和。

The disadvantage is that the size of the common mode becomes very large as the cutoff frequency is lowered, but there is no lower frequency limit caused by band pass or other factors. These inductors should have little effect on power factor correction circuits, switchers, or any other load. Again, this assumes little differential mode inductance within the common mode inductor.

共模截止频率很低的缺点是共模电感体积会很大，但通带和其它参数对共模的截止频率并没有最低频率限制。这些共模电感对功率校正电路、开关电源或其它负载影响很小。当然，得到这个结论的前提条件是共模电感只会产生很微小的差模电感。

§12.3 Estimate of Common Mode Load Impedance

§12.3 共模负载阻抗的估算

If the dc system is balanced, using the hot wire and a return wire, common mode inductors can be used without hindering the dc load. This assumes that the differential mode properties are low.

如果 DC 系统的电路是平衡的（同时使用火线和回线），那么就可以使用共模电感而不妨碍 DC 负载。当然这也是在假设共模电感的差模量较低的条件才成立的。

The common mode impedance of the typical nonisolated circuit in Figure 12.1, using the switcher as the common mode noise source, is as follows: G (the switcher and other elements) is now the noise source, and the circuit is drawn backward from the figure. This keeps the format used throughout this book of keeping the source, or line, to the left and the load to the right of each diagram. 在图 12.1 中典型的无隔离电路的共模阻抗如下（用开关电源作为共模噪声源）：G（开关管或其它器件）现在是噪声源，并把电路按图反过来。这样就保持了本书通用的电路形式：源和电源线在电路图左边，负载在右。

The storage capacitor is out of the circuit in Figure 12.2. The diodes and the transformer look capacitive, and the switcher inductor remains the same. The current probe measures the noise.

在图 12.2 中储能电容移出了电路，二极管和变压器看上去为容性，开关电源的电感保持不变。此时用电流探针测量噪声。

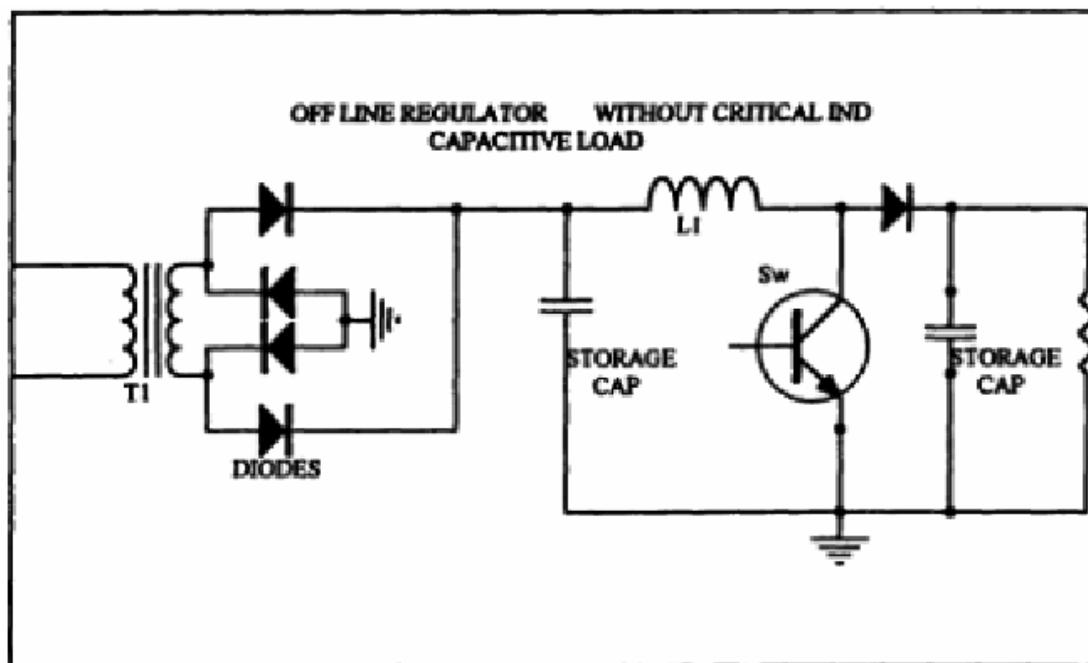


Figure 12.1 The switcher as the noise source in an off-line regulator without critical inductance and with capacitive load.

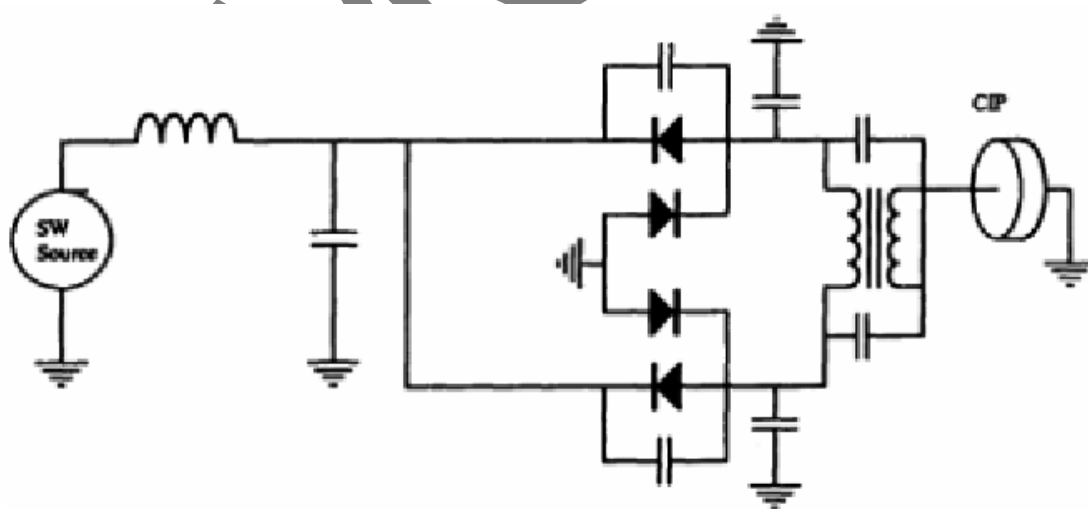


Figure 12.2 Capacitors around the power supply components.

Figure 12.3 shows the four capacitors across the diodes and the output transformer capacitor. If the transformer has a Faraday screen, the final capacitor is even smaller. All of this creates a common mode circuit impedance

that is much higher than the differential mode impedance. Paralleling the diodes, the circuit is as shown in Figure 12.4.

图 12.3 表示的是二极管和输出变压器的寄生电容。如果变压器有法拉第屏蔽罩，那么最后的那个电容器非常小。这些电容生成了远高于差模阻抗的共模电路阻抗。电路如 12.4 所示。

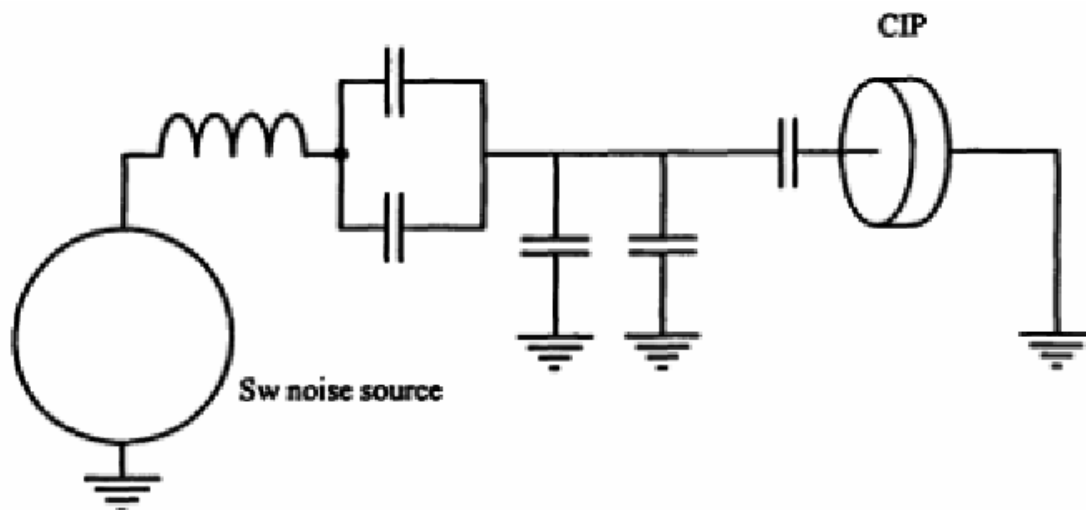


Figure 12.3 Power supply components reduced to capacitors.

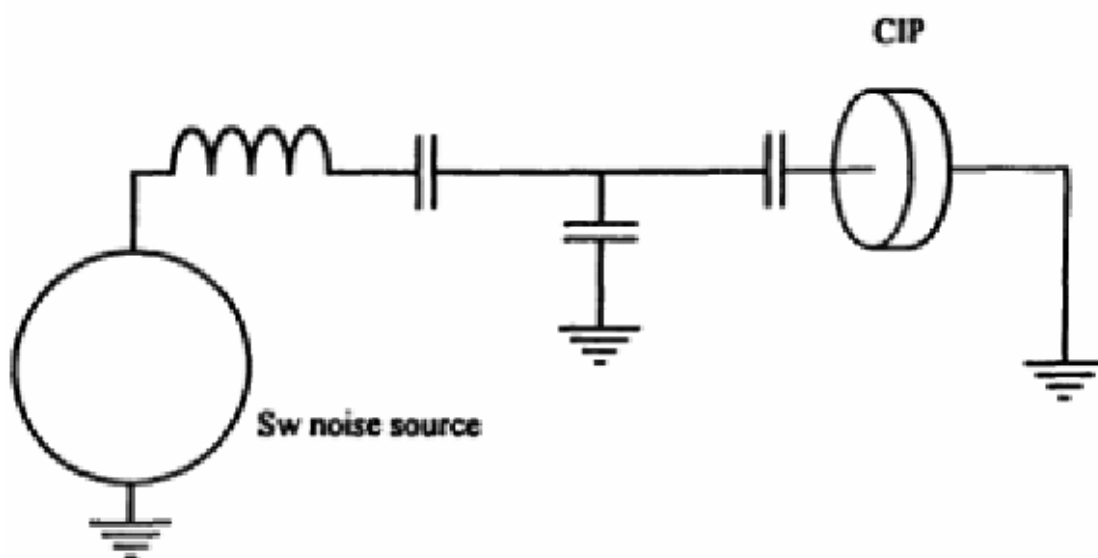


Figure 12.4 The final switcher reduced to capacitors.

If the circuit lacks a transformer, the diode capacitance to ground has a higher impedance than the current probe until the upper frequencies are reached (Figure 12.5).

如果电路没有变压器，那么直到上限频率以前二极管对地电容具有高于电流探针的高阻抗 (图 12.5)。

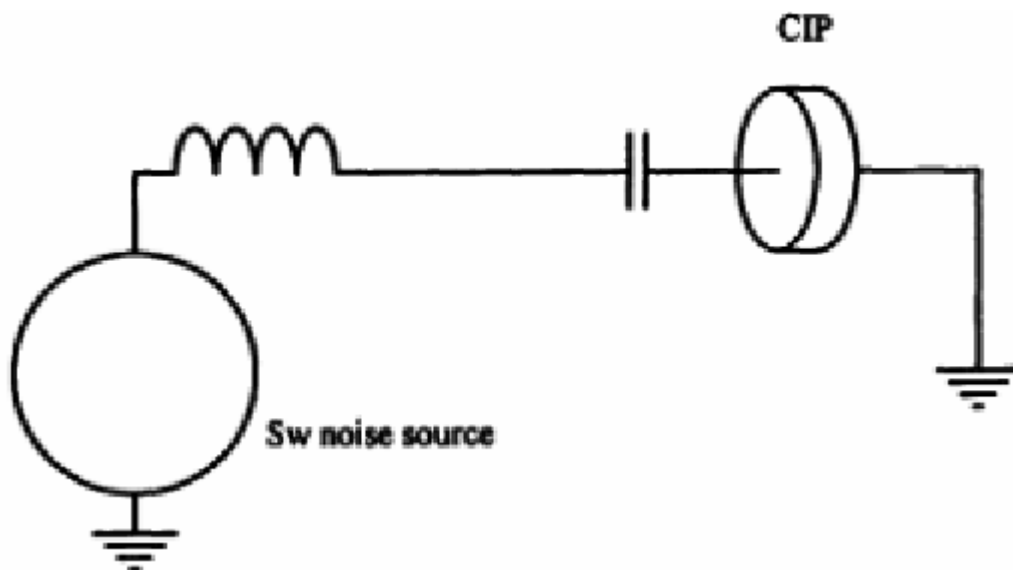


Figure 12.5 Simplified common mode load impedance.

Figure 12.5 shows that the common mode design impedance is higher than the differential mode impedance in most applications. This information allows the following technique. Calculate the cutoff frequency as before, and then determine the inductor and capacitor values with the same equations:

图 12.5 表明多数应用中共模设计阻抗大于差模阻抗，这就可以使用如下的设计方法。像以前一样计算截止频率，并用同样的表达式来计算电容和电感值。

$$L = \frac{R_d}{2pF_0} \quad C = \frac{1}{2pF_0 R_d}$$

where R_d is the design impedance and is the same as for the differential mode and F_0 is the cutoff frequency. If there is a leakage current specification, calculate the capacitor value of the capacitor to ground, or the specification may state the maximum value of capacitance to ground. Divide the needed value of capacitance by the maximum value, and multiply the inductor by this value. The cutoff frequency remains the same, but the impedance grows by the multiplier.

此处与差模情况相同 R_d 是设计阻抗， F_0 是截止频率。如果有漏电流规范，那么需要算出最大的对地电容值或规范已经给出了最大对地电容。将需要的电容值除以这个最大值得到一个倍数，并将电感乘以这个倍数，那么截止频率不变而阻抗等于原阻抗乘以倍数。

For example, the 400 Hz maximum to ground per line is 0.02 μF . In a single-phase circuit, two of these would be in parallel for the common mode application. With the design impedance of 10 Ω and a cutoff frequency of 3350 Hz, the common mode inductor would be

例如，400Hz 使用条件下每相线的最大对地电容为 0.02 μF 。在单相电路中，对共模情况相当于两个这样的电容并联。设计阻抗为 10 Ω ，且截止频率为 3350Hz，那么共模电感为：

$$\frac{10}{2p \cdot 3350} = 4.751 \times 10^{-4} = 475mH$$

and the capacitor would be

且电容为

$$\frac{1}{2p \cdot 3350 \times 10} = 4.751 \times 10^{-6} = 4.75 \text{mF}$$

which is much too large to meet the specification! An easier method of calculating the capacitor is to divide the calculated inductance value by the square of the impedance (10), or 100 here. Divide this value of capacitor by the maximum value of 0.04, the maximum allowed value of the capacitor to ground –a total of 0.02 times the two lines:

这个电容数值太大而不符合规范！一个简单的计算电容的方法就是将计算得到的电感值除以阻抗的平方，此处阻抗为 10 其平方为 100。接下来，将计算出的电容值除以最大允许电容值 0.04，（最大允许电容为 0.02，对于两条线加倍后为 0.04）：

$$\frac{4.751}{0.04} = 118.775$$

and multiply the inductance by this multiplier:

电容除后的结果乘以电感

$$118.775 \times 0.4751 \text{mH} = 56.43 \text{mH}$$

This gives an impedance of

得到新的阻抗为

$$\sqrt{\frac{56,430}{0.04}} = 1188 \Omega$$

but the cutoff frequency remains the same.

但是截止频率不变。

The value of inductance is excessive, and the common mode should be split into two sections. The value of F_0 will jump in value and make the two common mode inductors fall to reasonable values of inductance. This reduces the size, weight, and cost and gives better self-resonant frequency. The maximum capacitance to ground for each line section drops to 0.01, making the two in parallel 0.02 uF. **This technique of changing the values should not be used in differential mode.**

此电感的值过多，且此共模电感应分成两部分。 F_0 的值可以取合适的值以使得这两个共模电感取值比较合理。这可以减小电感的尺寸、重量和成本，并获得较好的自谐振频率。最大的对地电容降到 0.01，这样两个并联就是 0.02uF 了。注意：此改变数值的技术不能用在差模设计中。

Review of A Matrices

A 矩阵回顾

§13.1 Chain Matrix A: Transfer Functions

§13.1 A 矩阵链：转移函数

Matrices of various forms exist. Besides the A matrix, Z, Y, H, G, B, and now scatter parameters are used. The advantage of the A, or chain, matrix is that each element of a circuit can be chained, or in tandem, as the elements of the circuit appear, as in the circuit in Figure 13.1. R_1 and R_3 are series elements; R_2 and R_4 are shunt elements. Each of these resistors can make up a matrix, and each matrix can be multiplied by the following element. Continue through each following element as here:

矩阵有很多形式，目前正在使用的除了 A 矩阵外还有 Z、Y、H、G、B 和分散参数等矩阵。A 或矩阵链的优点是每个电路元件的矩阵就像电路中的元件一样，可以前后链接在一起。如图 13.1， R_1 和 R_3 是串联元件，而 R_2 和 R_4 是旁路元件。这些电阻每个都可以构成一个矩阵，且每个矩阵都可以与下一个相乘。按电路列出的矩阵链如下：

$$[R_1][R_2][R_3][R_4]$$

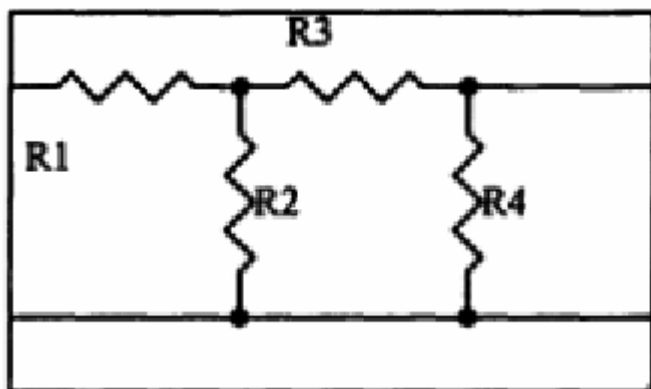


Figure 13.1 Matrix series and shunt elements.

Each matrix is formed by four elements, such as
每个矩阵由四个矩阵元组成，例如

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}$$

The series elements, R_1 and R_3 , make up the matrix element B:
串联元件， R_1 和 R_3 构成矩阵元 B：

$$\begin{bmatrix} 1 & R_1 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & R_3 \\ 0 & 1 \end{bmatrix}$$

and the shunt elements make up the matrix element C but are the reciprocals of their values:

傍路元件构成矩阵元 C，但是取的是元件参数的倒数：

$$\begin{bmatrix} 1 & 0 \\ \frac{1}{R_2} & 1 \end{bmatrix} \quad \begin{bmatrix} 1 & 0 \\ \frac{1}{R_4} & 1 \end{bmatrix}$$

These four matrices make up the following matrix equation:

这四个矩阵构成如下的矩阵等式：

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} 1 & R_1 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{R_2} & 1 \end{bmatrix} \begin{bmatrix} 1 & R_3 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{R_4} & 1 \end{bmatrix} \begin{bmatrix} V_o \\ I_o \end{bmatrix}$$

Matrix multiplication of the first two matrices and the last two together yields (for matrix multiplication, see Section 11.1)

前后两个矩阵各自相乘得（对于矩阵相乘方法，参见 11.1 节）

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} 1 + \frac{R_1}{R_2} & R_1 \\ \frac{1}{R_2} & 1 \end{bmatrix} \begin{bmatrix} 1 + \frac{R_3}{R_4} & R_3 \\ \frac{1}{R_4} & 1 \end{bmatrix} \begin{bmatrix} V_o \\ I_o \end{bmatrix}$$

If all the R are equal, the two 2×2 matrices reduce to

如果所有 R 都相等，这两个 2×2 矩阵可以简化成

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} 2 & R \\ \frac{1}{R} & 1 \end{bmatrix} \begin{bmatrix} 2 & R \\ \frac{1}{R} & 1 \end{bmatrix} \begin{bmatrix} V_o \\ I_o \end{bmatrix}$$

and the final matrix multiplication reduces to

最后矩阵相乘简化为

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} 5 & 3R \\ \frac{3}{R} & 2 \end{bmatrix} \begin{bmatrix} V_o \\ I_o \end{bmatrix}$$

If the load resistor is also R, then I_o is equal to V_o/R and the current and voltage follow:

如果负载电阻也是 R，那么 I_o 等于 V_o/R 且电流和电压为：

$$V_{in} = 5V_o + \frac{3RV_o}{R} = 8V_o$$

$$I_{in} = \frac{3V_o}{R} + \frac{2V_o}{R} = \frac{5V_o}{R}$$

The input impedance of the resistive pad is then $8R/5$, or $1.6R$. The only difference between the preceding text and the text that follows is that EMI filters use reactive components, adding J factors, or imaginary components, to the system.

计算得到这个阻性衰减器的输入阻抗是 $8R/5$ 或 $1.6R$ 。与上下文提到得 EMI 滤波器不同的是，滤波器使用电抗性元件时，需要加 J 参数，或称为虚数性元件。

§13.2 Review of A Matrices

§13.2 A 矩阵的回顾

This section reviews the chain matrix to take advantage of this tool to calculate insertion loss and other filter properties. These can be chained to form filter modules, such as Ts, π S, Ls, Cauer, and dissipative filters, along with their multiples. The matrix includes the load and source impedances, allowing direct calculation of the insertion loss.

本节将回顾矩阵链，并利用这种工具的优势来计算滤波器的插入损耗和其它特性。这些单元矩阵可以互相链接形成滤波器电路模块，如 T、 π L、考尔、损耗滤波器等。并且矩阵中含有负载和源阻抗，可以直接计算出插入损耗。

Knowledge of this section should allow easy additions by the reader as needed. All unit filters, except dissipative and Cauer filters, can be handled with four elements. These two also have four elements, but each term has two terms, one real and one imaginary, for a total of eight. Therefore, all filter equations must be equally complete so that each matrix solution can use the same form for each solution. This is like an overlay, and because each matrix fits the overlay, continuous solutions can be calculated. Any of these units can be described by the matrix equation, and thus these elements can be cascaded or chained to form an entirely new matrix transfer function. The user can place all of the elements as needed in tandem, and as long as the chain matrix does not run out of room (in terms of the computer program), these matrices can be chained ad infinitum.

本节的知识读者可以很容易地学习。除考尔和损耗滤波器外，所有的滤波器单元电路都可以用 4 个矩阵元表示。考尔和损耗滤波器单元也可以用四个矩阵元表示，但每项中又含有实数和虚数两项，这样总共就有 8 项。通常所有滤波器表达式都必须具有相同形式以便于每个矩阵解都具有相同的形式。这有些像计算机的覆载技术，因为每个矩阵的形式都符合标准，这样就可以通过计算机算出结果了。这些单元中的任何单元都可以用矩阵表达式描述，并且这些元矩阵可以前后层叠并形成新的传递函数矩阵。只要矩阵链不超出限制（按计算机程序的不同而不同），使用者就可以按需要前后排布矩阵，这些矩阵可以无限链接下去。

The filter designer must know the voltage, current, required insertion loss, operating frequency of the power line, and other information about the load. In

these equations our only concern is the filter loss at a known frequency, such as -30 dB at 14 kHz. Often the required filter loss is specified by an electromagnetic interference (EMI) test laboratory after running the proper tests on the unit. In other cases it is only a good educated guess by the equipment or power supply designer using equations given in earlier chapters. The filter designer's goal is to meet the specified needed loss with some added headroom. From the final matrix of all the combined elements, the loss at a given frequency can be calculated with an estimated load and source impedance. The government normally specifies the insertion loss of a filter at 50 Ω load and source impedance in the 220A specification. The designer can insert these values for any load and source needed. In our case, the designer picks a filter arrangement, such as a double T, and uses a program to find the cutoff frequency needed to obtain the loss. Such programs as GOAL-SEEKER, a shareware program, or any other program, such as the newer Lotus What If programs, can be used. Again, these programs are used to detect the cutoff frequency, giving the needed loss with about 6 dB headroom. If the cutoff frequency F_0 is too low, cutting too deep into the frequency band pass (10 times the line frequency is suggested), another stage must be added (here another T). GOAL-SEEKER, or whatever method used to iterate between the needed loss and the cutoff frequency, is then used again to find the new, higher cutoff frequency to ensure that the filter is not too close to the band pass, as before. Usually, the band pass should be at least 10 times the line frequency.

滤波器设计者必须了解电压、电流、所需插损、电源线工作频率和其它有关负载的信息。在这些参数中此处我们只关心在已知频率下滤波器的损耗，如在 14kHz 损耗为 -30dB。通常滤波器的损耗是由 EMI 测试实验室在对滤波器测试后标定的。但一般情况下，设计之初插损的计算仅仅是由设备或电源设计者利用我们前面章节的公式进行合理的估算。此时滤波器设计者的目标是满足规格书的损耗要求并适当增加余量。通过综合各个元件计算所得的最终矩阵，再考虑负载和源阻抗的估计值，就可以计算给出所需频率下的滤波器损耗。在 220A 规范中认证机构通常规定滤波器的插入损耗是在源和负载阻抗为 50 Ω 的条件下测量的。也就是说，对于任何源和负载应用情况，设计者都可以使用这些源和负载值。在我们的例子中，滤波器设计者选择了一种滤波器排列方式，如双 T 型，并使用程序计算出需要的截止频率和滤波器损耗。此类程序有共享软件 GOAL-SEEKER 或其它软件如最新的 Lotus What If 软件等软件可以使用。这些软件可以计算出截止频率并给出 6dB 的插损余量。如果截止频率 F_0 太低，导致其切入通带的频率（建议 10 倍于电源线频率）区域太深，那么就需要增加另外一节电路（此处增加的是另一节 T 电路）。用来在需要的损耗和截止频率之间迭代的 GOAL-SEEKER 或其它方法同样也可用来计算新的较高的截止频率以保证滤波器截止频率不会与通带频率太接近。通常，通带频率至少是电源线频率的 10 倍。

All the matrices listed here are 2×2 square matrices giving four elements. As the number of elements or stages grows, the complexity of the terms grows, not the number of elements. Thus, a simple single element has four terms, but the terms are easily calculated; a 4L also has four terms, but the terms may be algebraically complex. Also, the terms for Cauer and dissipative filters are made up of both real and imaginary terms. Thus, the matrix may be four elements but

can have eight terms. All the layouts should be the same to use the same matrix equation solutions, such as

此处所有列出的 2×2 矩阵具有 4 个矩阵元。当元件或滤波器节数增加时，矩阵元的数目没有变化但每个矩阵元变复杂了。因此，一个单一的元件有 4 个矩阵元，但每个矩阵元很容易计算；而 4L 电路也只有 4 个矩阵元，但每个矩阵元会是一个复杂的数学式。同样，虽考尔和损耗滤波器的矩阵元含有实数和虚数项。但它们的矩阵也是 4 个矩阵元，只是因为复数的原因所以共有 8 项。所有矩阵都使用相同的排布形式，如

$$\begin{bmatrix} A + JB & C + JD \\ E + JH & G + JF \end{bmatrix} \quad (\text{原文为: } \begin{bmatrix} A + JB & C + JD \\ E + JH & G + JH \end{bmatrix} \text{ 译者注}) \quad (13.1)$$

where A, C, E, and G are real and B, D, F, and H are imaginary and where A through H may be quite complex algebraically. The determinant of the chain matrix, δ must always equal 1, and the imaginary term is 0. Closer counts here, though, as in the imaginary reading of 3.8×10^{-7} , is near enough to zero to qualify. Other cases creating answers close to 1 and 0 are caused by changing from one style of matrix to another. Some networks have parallel branches, as in the dissipative filter. The two branches were each initially set up using A matrices, and each was then converted to Y matrices (admittance matrices)-These were then added and converted back to the A matrix form. This process often creates rounding errors. The δ of the determinant is slightly off from 1 and leads to an imaginary term different from 0. That is,

此处 A、C、E 和 G 为实数，B、D、F 和 H 为虚数项，且从 A 到 H 都可能是复杂的代数式。在矩阵链的行列式中， δ 必须总为 1，虚数项为 0。如尽管虚数读数为 3.8×10^{-7} ，但此处的近似数已经十分接近 0 值的限制。在其它的例子中因为更换矩阵类型的原因解会接近 1 和 0。一些电路网络如损耗滤波器中含有并联分支，损耗滤波器中的这两个分支最初按 A 矩阵类型设置，然后把每个 A 矩阵转换成 Y 矩阵（导纳矩阵）—这两个矩阵相加后再转换回 A 矩阵形式。这个过程常常会产生舍入误差。行列式的 δ 会稍微偏离 1，复数项也会稍微异于 0 值。行列式的迹为：

$$(A + JB)(G + JH) - (C + JD)(E + JF) \quad (13.2)$$

This is true for all the matrices in the chain, as well as the resultant matrix, except for the dissipative, Cauer, and other filters because of matrix conversions, adding ambiguity to some elements. The order of progression of the matrices is in the same order of progression in which entire filter types are laid out. The order cannot be changed without arriving at an incorrect answer, but combining them can be worked in any order as long as adjacent matrices are combined or reduced.

除了由于矩阵转换使得某些矩阵元值具有不确定性的损耗和考尔滤波器外，对链路中的所有矩阵以及组合矩阵都是如此。虽然矩阵的级数与整个滤波器排布具有相同的级数。但是可以通过合并相邻的矩阵来任意变化矩阵的级数。

The solution of a two-element column matrix composed of the two matrices as before is

由前面提到的两个矩阵构成的两矩阵元的列矩阵的解为

$$\begin{pmatrix} V_{in} \\ I_{in} \end{pmatrix} = \begin{pmatrix} A + JB & C + JD \\ E + JF & G + JH \end{pmatrix} \begin{pmatrix} K + JL & M + JN \\ P + JQ & R + JS \end{pmatrix} \begin{pmatrix} V_o \\ I_o \end{pmatrix} \quad (13.3)$$

$$\begin{pmatrix} V_{in} \\ I_{in} \end{pmatrix} = \begin{pmatrix} (A + JB)(K + JL) + (C + JD)(P + JQ) & (A + JB)(M + JN) + (C + JD)(R + JS) \\ (E + JF)(K + JL) + (G + JH)(P + JQ) & (E + JF)(M + JN) + (G + JH)(R + JS) \end{pmatrix} \begin{pmatrix} V_o \\ I_o \end{pmatrix} \quad (13.4)$$

The first term is equal to

第一项等于

$$AK + JAL + JBK - BL + CP + JCQ + JDP - DQ \quad (13.5)$$

These can be separated into real and imaginary components:

可以将实数部分和虚数部分分开

$$(AK - BL + CP - DQ) + J(AL + BK + CQ + DP) \quad (13.6)$$

The same follows for the remainder of the terms. All the value of A through S reduce either to numbers or to basic algebraic equations. These filters are based on two terms, K and R_d , where K is the normalized frequency, so that these can be plotted, and R_d is the design impedance. The first element just rendered reduces to a new $A + JB$, and so do the remainder of the elements. The new combined matrix is:

对剩余项做同样处理。这样所有通过 S 得到的 A 矩阵的值都简化为数值或基本的代数式。计算中这些滤波器都基于两个参数, K 和 R_d , 此处 K 是归一化频率 (这样就比较容易画出曲线), R_d 为设计阻抗。第一项简化成新的 $A + JB$ 项, 对其余的矩阵元也做同样处理, 得到新矩阵为:

$$\begin{pmatrix} V_{in} \\ I_{in} \end{pmatrix} = \begin{pmatrix} A' + JB' & C' + JD' \\ E' + JF' & G' + JH' \end{pmatrix} \begin{pmatrix} V_o \\ I_o \end{pmatrix} \quad (13.7)$$

Again, the determinant of the matrix is 1, which means that the J terms vanish for those derived purely via A matrix components:

同样, 矩阵行列式结果为 1, 这意味着通过 A 矩阵元件产生的虚数项被消去了。

$$A'G' - B'H' - C'E' + D'F' = 1 \quad (13.8)$$

$$J \cdot (A'H' + B'G' - C'F' - D'E') = 0$$

Note, as stated before, that close counts for the J term, equaling zero on some of the derived matrices as a result of rounding errors, are created especially when moving between different matrices, such as converting to Y matrices (doing some addition) and then converting back to the A matrix form. Also note that $V_o/R_l = I_{in}$. If this is the final form after multiplying all the matrices, this can be transformed to complex algebra by

注意到, 如前所述虚数项的近似值虽应在误差范围内等于零, 但是由于在不同类型矩阵之

间转换（如转换为 Y 矩阵做加法后并再转换回 A 矩阵形式）产生了不为零的虚数项。还应注意注意到 $V_o/R_l = I_{in}$ 的等式，如果这是所有矩阵相乘后的最终结果，那么此式可以转换成复杂的代数式：

$$V_i = \frac{V_o(R_l(A' + JB') + C' + jD')}{R_l}$$

$$\frac{V_i}{V_o} = \frac{R_l(A' + JB') + C' + jD'}{R_l} \quad (13.8)$$

$$\frac{V_i}{V_o} = \frac{R_l A' + C' + J(B' R_l + D')}{R_l}$$

So that the voltage ratio

所以电压比为

$$\frac{V_o}{V_i} = \frac{R_l}{R_l A' + C' + J(B' R_l + D')} \quad (13.10)$$

Dropping the primes for clarity,

为简便，按最初的形式来改写上式（去掉“'”）

$$\frac{V_o}{V_i} = \frac{R_l}{R_l A + C + J(B R_l + D)}$$

$$\frac{V_o}{V_i} = \frac{R_l}{\sqrt{(A R_l + C)^2 + (B R_l + D)^2}}$$

$$\text{(原文为 } \frac{V_o}{V_i} = \frac{R_l}{\sqrt{(A R_l + C)^2 + B R_l + D)^2} \text{ , 译者注。)}$$

This voltage ration is compared with the voltage ratio of the source and load impedances without the filter (Figure 13.2):

此电压比是在没有滤波器时的源和负载的电压比（图 13.2）：

$$\frac{R_s + R_l}{R_l} \frac{R_l}{\sqrt{(A R_l + C)^2 + (B R_l + D)^2}} = \text{insertion loss} \quad (13.11)$$

where R_s and R_l are the source and load impedances. The decibel loss is given by

此处 R_s 和 R_l 是源和负载阻抗，分贝损耗为：

$$20\log \frac{R_s + R_l}{\sqrt{(AR_l + C)^2 + (BR_l + D)^2}} \quad (13.12a)$$

or

$$20\log(R_s + R_l) - 20\log \sqrt{(AR_l + C)^2 + (BR_l + D)^2} \quad (13.12b)$$

or

$$20\log(R_s + R_l) - 10\log[(AR_l + C)^2 + (BR_l + D)^2] \quad (13.12c)$$

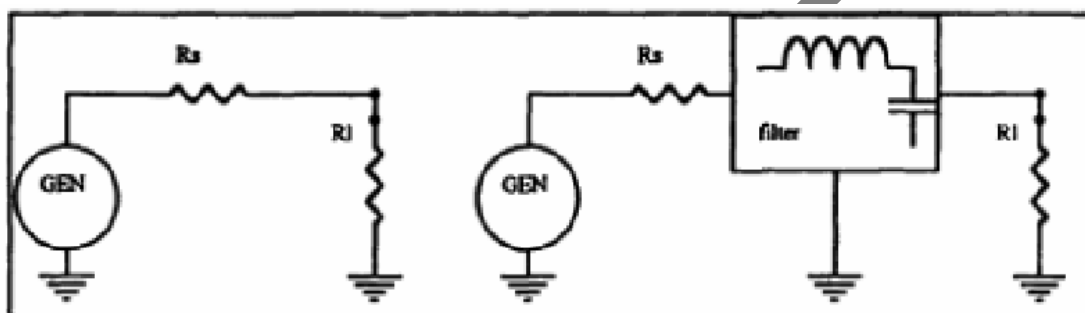


Figure 13.2 The insertion loss with and without the filter.

The angel of lag is

滞后角为

$$\tan^{-1} \frac{BR_l + D}{AR_l + C} \quad (13.13)$$

Engineering manuals and the Institute of Electrical and Electronics Engineers literature confirm many reasonably priced programs (others are not so reasonable) are available that plot, list decibel losses, give phase angles, and so on, but I know of no program that calculates the value of the components needed for a specific loss other than for conventional filter design techniques in which known input and output impedances are mandatory. Some use these programs to back-engineer an EMI filter by changing the component values until their goal of decibel loss at a particular frequency is reached. This, and most other similar methods, gives random values of components that yield the needed loss for the 50 Ω test setup but can do strange things to the band pass in the real world. This method can also provide a resonant rise at a low harmonic of the line frequency, oscillate, heat the filter, or present such a low input impedance that the circuit breaker may trip on turn-on.

《工程师指南》和 IEEE 都确定了一些定价合理的软件（其它的定价就不怎么合理了），这些软件可以画出和列出损耗，并给出相位角等参数。但据我了解，没有软件能计算出要达到规定的插损所需的元件参数，而现有软件只具有根据固定的输入和输出阻抗来设计滤波器的常规滤波器设计技术。一些人会使用这些软件来帮助更换元件的值，直到他们所要求

的特殊频率点的损耗达到要求为止。这种方法和其它类似方法一样会给出能在 $50\ \Omega$ 测试设置条件下达到所需插损的元件的值，但是在实际应用中会对通带产生奇特的影响。因为这种方法会在低频谐波的频率点上产生谐振并导致增益、产生振荡，使滤波器变热或表现出低输入阻抗使得电路断路器误开启。

If the inductances and capacitors are pure, the series element of inductive reactance is placed in the $C+JD$ and any shunt or parallel element reciprocal impedance is placed in $E+JF$. A simple L formed with a series inductor followed by a parallel or shunt capacitor forms such a small chain matrix. Note that C and E are both 0, because their small values of ESR and DCR are neglected-or treated as pure-and the inductor faces the line and the capacitor faces the load. 如果把电感和电容做理想元件处理，那么它们的串联感抗则要置于 $C+JD$ 项中，任何傍路或并联元件的阻抗的倒数会置于 $E+JF$ 项中。一个串联电感后接并联电容的简单的 L 型滤波器会具有这样一个小矩阵链，注意 C 和 E 都为 0，这是因为忽略了它们的很小的 ESR 和 DCR 值，把它们当成理想元件进行了处理。如电感面向电源线，电容面向负载的 L 型滤波器，则

$$\begin{bmatrix} 1+J_o & 0+JX_l \\ 0+J_o & 1+J_o \end{bmatrix} \begin{bmatrix} 1+J_o & 0+J_o \\ 0+\frac{J}{X_c} & 1+J_o \end{bmatrix} \begin{bmatrix} V_o \\ I_o \end{bmatrix} \quad (13.14)$$

Eliminating the unnecessary zeros,
消去无用的零值，

$$\begin{bmatrix} 1 & JX_l \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \frac{1}{J} & 0 \\ \frac{J}{X_c} & 1 \end{bmatrix} \begin{bmatrix} V_o \\ I_o \end{bmatrix} \quad (13.15)$$

The new matrix becomes
新矩阵变成

$$\begin{bmatrix} V_i \\ I_i \end{bmatrix} = \begin{bmatrix} 1-\frac{X_l}{X_c} & JX_l \\ \frac{J}{X_c} & 1 \end{bmatrix} \begin{bmatrix} V_o \\ I_o \end{bmatrix} \quad (13.16)$$

This might look bad, but the first term reduces to $1-K^2$, as follows.
这虽看上去较差，但是后面会把第一项简化成 $1-K^2$ 。

The inductance and capacitance equations are
电感和电容的表达式为

$$L = \frac{R_d}{2pF_0} \quad C = \frac{1}{2pF_0 R_d} \quad (13.17)$$

The inductive reactance using Equation 13.17:

应用等式 13.17，感抗为

$$X_l = 2pFL = \frac{2pFR_d}{2pF_0} = \frac{FR_d}{F_0} \quad (13.18)$$

The capacitive reactance, also using Equation (13.17):

同样应用等式 13.17，容抗为：

$$X_c = \frac{1}{2pFC} = \frac{2pF_0R_d}{2pF} = \frac{F_0R_d}{F} \quad (13.19)$$

but

$$F = KF_0$$

The inductive and capacitive reactance becomes

容抗和感抗变为

$$X_l = KR_d \quad X_c = \frac{R_d}{K} \quad (13.20)$$

K is the normalized frequency, R_d is the design impedance, and F_0 is the cutoff frequency.

K 为归一化频率， R_d 是设计阻抗， F_0 为截止频率。

The matrix (13.16) is

矩阵 (13.16) 为

$$\begin{bmatrix} V_i \\ I_i \end{bmatrix} = \begin{bmatrix} 1-K^2 & JKR_d \\ J\frac{K}{R_d} & 1 \end{bmatrix} \begin{bmatrix} V_o \\ I_o \end{bmatrix} \quad (13.21)$$

Note that terms 1 and 4 are real and resistive and 2 and 3 are imaginary. Also note that this matrix yields a δ value of 1. What happens if the order is changed? This places the shunt capacitor on the line side and the series inductor facing the load.

注意 1 项和 4 项是实数则为阻性，2 项和 3 项为虚数。同样，此矩阵的 δ 值为 1。如果此滤波器的元件次序发生变化会如何？现将傍路电容置于电源线侧并将串联电感置于面向负载侧。

$$\begin{bmatrix} V_i \\ I_i \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ J & 1 \end{bmatrix} \begin{bmatrix} 1 & JX_l \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_o \\ I_o \end{bmatrix}$$

Substituting these values for X_l and X_c ,

将的 X_L 和 X_C 值带入上式

$$\begin{bmatrix} V_i \\ I_i \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{JK}{R_d} & 1 \end{bmatrix} \begin{bmatrix} 1 & JKR_d \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_o \\ I_o \end{bmatrix}$$

Multiply the two matrices:

将两矩阵相乘，得

$$\begin{bmatrix} V_i \\ I_i \end{bmatrix} = \begin{bmatrix} 1 & JKR_d \\ \frac{JK}{R_d} & 1 - K^2 \end{bmatrix} \begin{bmatrix} V_o \\ I_o \end{bmatrix} \quad (13.22)$$

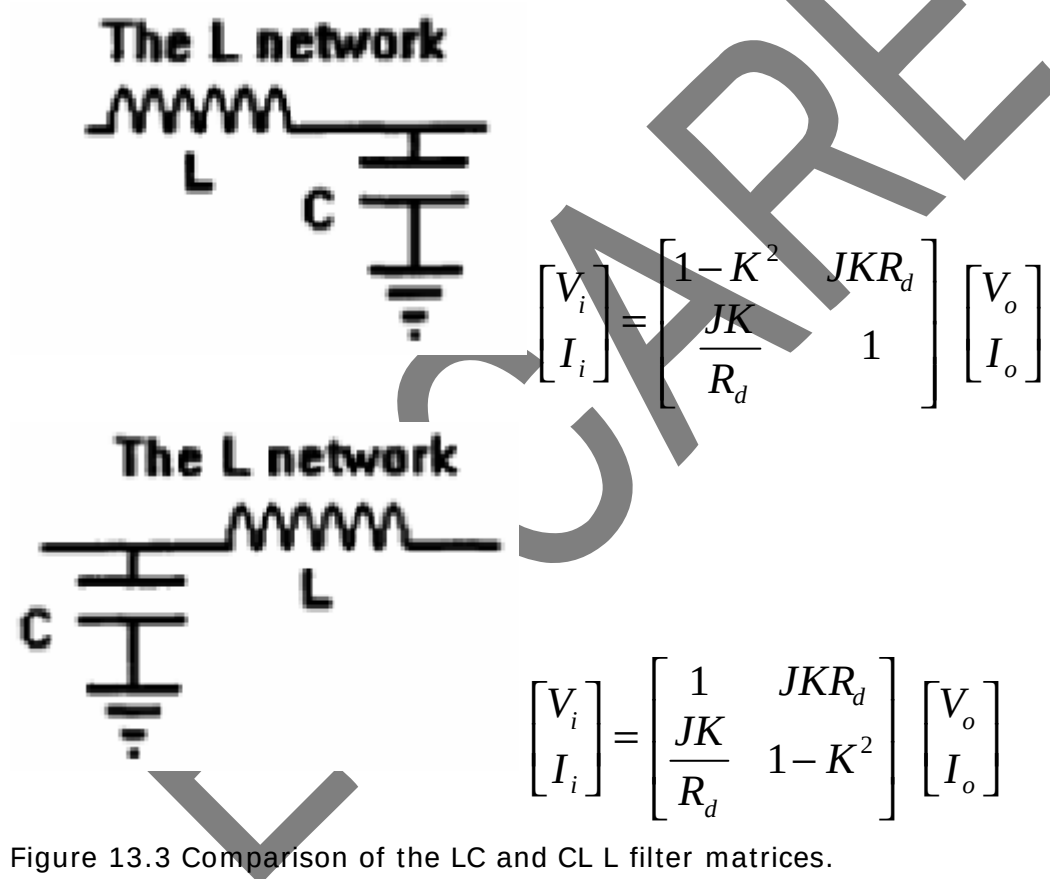


Figure 13.3 Comparison of the LC and CL L filter matrices.

Note the difference in the two answers, showing what happens when elements are processed in the wrong order, by comparing Equations (13.21) and (13.22) (Figure 13.3). Either answer is correct, depending on what element the designer wants facing the line or the load. Most EMI filter designers want the inductor on the line side, especially for 461 specifications or any specification requiring high insertion losses at frequencies near 14 kHz.

通过对比 (13.21) 和 (13.22) (图 13.3) 这两个解的差异可以看出，如果元件顺序安装错误会产生什么影响。当然两种方式都是正确的，不同之处只是看滤波器设计者期望什么元件对应电源线和负载端口。多数滤波器设计者会希望电感位于电源线侧，尤其是为满足

461 规范或其它在 14kHz 附近频率点需要高插入损耗的要求时。

A multiple L of the type in Equation (13.21) with the inductor on the line side can be formed by

电感位于电源线侧的双 L 型滤波器（每个 L 型都是（13.21）表示的类型），矩阵表达式如下

$$\begin{bmatrix} V_i \\ I_i \end{bmatrix} = \begin{bmatrix} 1-K^2 & JKR_d \\ J\frac{K}{R_d} & 1 \end{bmatrix} \begin{bmatrix} 1-K^2 & JKR_d \\ J\frac{K}{R_d} & 1 \end{bmatrix} \begin{bmatrix} V_o \\ I_o \end{bmatrix} \quad (13.23)$$

This reduces to

此方程简化为

$$\begin{bmatrix} V_i \\ I_i \end{bmatrix} = \begin{bmatrix} 1-3K^2+4K^4 & JKR_d(2-K^2) \\ \frac{JK(2-K^2)}{R_d} & 1-K^2 \end{bmatrix} \begin{bmatrix} V_o \\ I_o \end{bmatrix} \quad (13.24)$$

The δ of the matrix is

此矩阵的 δ 为

$$\begin{aligned} & [1-3K^2+K^4](1-K^2) - J^2K^2(2-K^2) \\ & [1-3K^2+K^4-K^2+3K^4-K^6] + K^2(4-4K^2+K^4) \\ & (1-4K^2+4K^4-K^6) + (4K^2-4K^4+K^6) = 1 \end{aligned}$$

If the cutoff frequency F_0 is 4000 and the frequency of interest is 400, then $K=400/4000=0.1$, and if $R=20$, the preceding values would be

如果截止频率为 4000，我们感兴趣的频率是 400，那么 $K=400/4000=0.1$ ，如果 $R=20$ ，前述的值将为

$$\begin{bmatrix} V_i \\ I_i \end{bmatrix} = \begin{bmatrix} 0.9701 & 3.98J \\ 0.00995J & 0.99 \end{bmatrix} \begin{bmatrix} V_o \\ I_o \end{bmatrix}$$

If the load is also 20, then $I_o=V_o/R_l$ and

如果负载也是 20，那么 $I_o=V_o/R_l$ 并且

$$V_i = V_o \left(0.9701 + \frac{3.98J}{20} \right)$$

$$V_i = \frac{V_o}{20} (19.402 + 3.98J)$$

and

$$I_i = V_o \left(0.0099J + \frac{0.99}{20} \right)$$

$$I_i = \frac{V_o}{20} (0.199J + 0.99)$$

Then,

$$Z_i = \frac{19.402 + 3.98J}{0.99 - 0.199J} \frac{0.99 - 0.199J}{0.99 - 0.199J} = \frac{20 + 0.0792J}{1.0197}$$

Z_i equals 19.614 at 13.613 minutes.

在 13.613 弧度, Z_i 等于 19.614

The value of the impedance is not too far from the expected 20, and there is in essence on phase angle.

可以看出阻抗的值并没有太远离预计的值 20, 并且相位角也无明显变化。

Various values of K can be plotted, or any one frequency can be quickly checked. The main advantage is that the filter element values are given for the required insertion loss. The various filter sections needed are listed for each term of the matrix, and the method for designing other units is included in this chapter. All the equations are listed to follow the format of Equation (13.7) without the primes:

使用此方法可以画出不同 K 值的数据曲线, 同样可以查找任何频率的值。其主要的优点是, 对于具体的差损要求可以得到滤波器元件的参数。滤波器不同部分都在矩阵的每一项中列出了, 并且设计其它单元的设计方法也包含在本章的内容中了。以后列出的所有等式都与 (13.7) 的等式相同, 只是去掉了原来的标记“'”。

$$\begin{bmatrix} V_i \\ I_i \end{bmatrix} = \begin{bmatrix} A + JB & C + JD \\ E + JF & G + JH \end{bmatrix} \begin{bmatrix} V_o \\ I_o \end{bmatrix} \quad (13.25)$$

14

Filter Design Technique

滤波器设计技术

Here we discuss how to build the matrices for all the filter elements in the following list. The names can be changed if a designer wishes to build these filters into a computer program. These names are only those I used initially in my programming.

此处我们将讨论如何去为下列滤波器单元建立矩阵。如果滤波器设计者想在计算机软件中建立这些滤波器模型，那么这些名字是可以修改的。其实这些名字只是最初用在我的软件中的名字。

1. Unit matrix
2. R_s matrix
3. LINESIM matrix
4. LISN matrix
5. DIN and DOUT matrices
6. RCSHU matrix
7. LSER matrix and CSHU matrix
8. L filter
9. π filter
10. T filter
11. Cauer filter and matrix

§14.1 The Unit Matrix

§14.1 单元矩阵

The simplest matrix is the unit matrix. This is the equivalent of scalar multiplication by 1. The unit requires no input. Verify that all the unused elements of the matrix field contain unit elements, not other filter elements, because these other elements in these sections will give erroneous higher losses, making the filter appear to have the required specified losses even though it is well out of the required specification.

最简单的矩阵就是单元矩阵。它等同于标量的倍数 1。单元矩阵要求没有输入。在矩阵域中所有未使用元件的矩阵元都置为单元矩阵元，而没有其它的滤波器矩阵元，这是因为如果在没有元件处使用这些其它的滤波器矩阵元会错误地给出较高地损耗，结果是虽然实际上还没有达到损耗要求，但计算出的滤波器还是表现为已经具有了规定的损耗。

The value are

单元矩阵的值为

$$\begin{bmatrix} 1 + j0 & 0 + j0 \\ 0 + j0 & 1 + j0 \end{bmatrix} \quad (14.1)$$

In reality, the unit matrix is a square diagonal matrix, as follows:

实际上，单元矩阵是一种四方对角矩阵，如下：

$$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$$

The off-diagonals are all zero, and again, this is like multiplying the matrix field by 1.

可以看出单元矩阵的反斜对角元均为零，这个矩阵的作用类似于在矩阵域中乘 1 的行为。

§14.2 The R_s Matrix

§14.2 R_s 矩阵

The value needed for an R_s filter (Figure 14.1) comes from the ‘Common Terms’ section, and is used for the input-side line impedance R_s . This term is the lower frequency line resistance or source impedance. This is fine for frequencies under 100 kHz, at which a skin effect is not operative and the filter is being designed for insertion losses around 14 kHz.

R_s 滤波器需要的值来自于“共模项”的章节（图 14.1），并会在确定输入电源线侧阻抗时用到 R_s 这个值。此项是低频率下的线阻抗或源阻抗。这会在频率低于 100kHz 时效果较好（此时滤波器是为在 14kHz 频率附近的插损设计的），因为在此频率下趋肤效应还没有产生。

Most of the various groups who have tested power lines have agreed that the line impedances are around 4 Ω at 10 kHz. Here, the value of 4 Ω is assigned. 许多测试过电源线的组织都认为，电源线阻抗在 10kHz 时约为 4 Ω 。因此此处把 R_s 赋值为 4 Ω 。

$$R_s = 4\Omega = \begin{bmatrix} 1 + j0 & 4 + j0 \\ 0 + j0 & 1 + j0 \end{bmatrix} \quad (14.2)$$

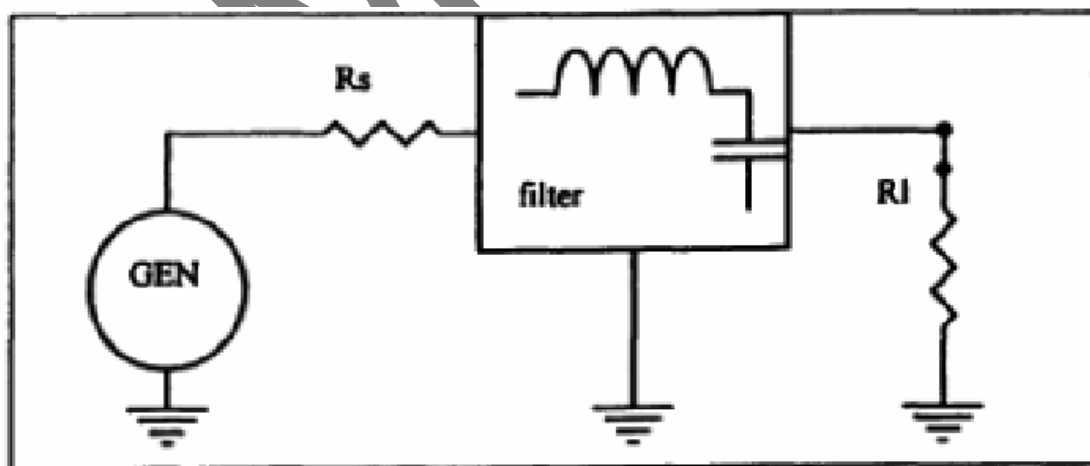


Figure 14.1 The R_s matrix

which is reduced to the following (but all the matrices must have the eight terms so that they can overlay the equation format and the solutions may be repeated whatever the matrix placed in the equation):

上面的矩阵简化为如下形式（但是所有的矩阵都必须有 8 项，这样它们都可以符合等式的通用形式，并且无论矩阵是否置于表达式中都可以求解）：

$$\begin{bmatrix} 1 & 4 \\ 0 & 1 \end{bmatrix} \quad (14.3)$$

No further information is needed for the unit matrix, which describes the line, not the filter.

对于描述电源线而不是滤波器的单元矩阵，实际上并不再需要其它的输入信息了。

§14.3 The LINESIM Matrix

§14.3 LINESIM 矩阵

The LINESIM matrix is used to match a known line or the output impedance of a dc power supply (Figure 14.2). The small series resistor is the value of R_s from the ‘Common Terms,’ but the value of the shunt resistor R_{hf} and the series inductor L_1 must be given. R_s , K , and F_0 should be available from the ‘Common Terms’ area and are needed here. R_{hf} , the high shunt resistance, and L_1 must be known. R_s acts as the low-value series impedance of the source. A different symbol can be used. This value must be provided if R_s is not used.

LINESIM 矩阵是用来与已知的电源线或 DC 电源的输出阻抗（图 14.2）相配的。小的串联阻抗是源自于“共模项”的 R_s 值，但是旁路电阻 R_{hf} 和串联电感 L_1 也同样需要给出。此处所需的 R_s 、 K 和 F_0 都可以通过“共模项”获得。但还需要知道高旁路阻抗 R_{hf} 和 L_1 。 R_s 为低阻值的串联源阻抗，这个值是必须提供的。

The frequency of interest is
感兴趣的频率为

$$F = KF_0 \quad (14.4)$$

This makes X_l equal to
这使得 X_l 等于

$$X_l = 2pFL = 2pKF_0L$$

R_s , R_{hf} , and L_1 are given so that values can be inserted directly into the matrix, so that the line simulation network impedance follows the normalized frequency. Thus, as K varies, the inductive reactance of this network varies along with the filter.

R_s , R_{hf} , 和 L_1 是已知的，所以可以直接将它们的值插入矩阵中，因此线模拟网络阻抗由归一化频率决定。因此，当 K 变化时，此网络的感抗同滤波器一起发生变化。

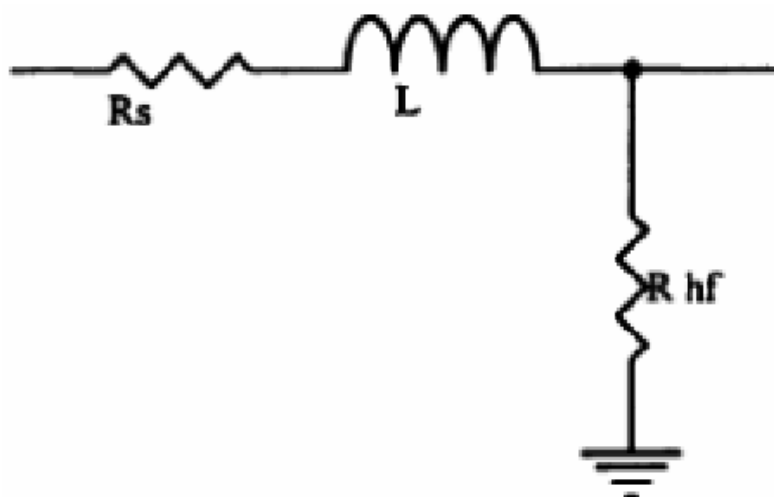


Figure 14.2 The LINESIM network.

The LINESIM matrix is

LINESIM 矩阵为

$$\begin{bmatrix} V_i \\ I_i \end{bmatrix} = \begin{bmatrix} \frac{R_{hf} + R_s}{R_{hf}} + \frac{JX_L}{R_{hf}} & R_s + JX_L \\ \frac{1}{R_{hf}} + J0 & 1 + J0 \end{bmatrix} \begin{bmatrix} V_o \\ I_o \end{bmatrix} \quad (14.5)$$

For example, F_0 is 4000, R_s is 4, R_{hf} is 50, L is 90 uH, and K floats, so it can be plotted.

例如 F_0 为 4000、 R_s 为 4、 R_{hf} 为 50、 L 为 90 uH、并带入 K ，这样它就可以表示出来了。

$X_L = 2.262K$, so the matrix becomes

$X_L = 2.262K$ ，因此矩阵变成

$$\begin{bmatrix} 1.08 + 0.0452JK & 4 + 2.262JK \\ 0.02 + 0J & 1 + 0J \end{bmatrix} \quad (14.6)$$

When this matrix is multiplied by the others in the series, the various values of K can be plotted. The LINESIM network is not part of the filter and accounts for the line impedance.

当此矩阵与后面其它的矩阵相乘时，此时可以画出随 K 变化的值。此 LINESIM 矩阵并不是滤波器的一部分，而是要计算到电源线阻抗中去。

§14.4 The LISN Matrix

§14.4 LISN 矩阵

The input section formed by R_{in} and C_{in} is in series shunt across the line. The midsection is made up of one inductor in series, L_1 . The output section, with R_o

and C_o in series shunt, is also across the line. All these values must be known. The initial values are from a standard LISN but can be changed. The default values in any of these sections can always be used. The engineer can input the main LISN values used repeatedly and save these values so that this information need not be reentered each time this LISN is used. If more than one LISN is used, several LISNs can be added by copying the equations into each new section and changing the known values. These would be called LISN1, LISN2, and so on.

LISN 由 R_{in} 和 C_{in} 串联并于线间构成了输入部分。其中心部分一个串联电感 L_1 ，由 R_o 和 C_o 组成的输出部分同样也并于线间。这些值都是计算需要的，虽然从标准 LISN 可以得到最初的值，但是实际上这些值与当初相比可能会改变。工程师可以输入主 LISN 值并保存，这样就可以重复使用而不需要每次输入了。如果使用了多个 LISN，可以拷贝原来的表达式到新的式子中，并修改相应的部分。当然可以将这些 LISN 命名为 LISN1、LISN2 等等。

LISN units are used by electromagnetic interference (EMI) test laboratories and are often required for the various test specifications (Figure 14.3). If the test specification calls for an LISN, this matrix can be handy for the design of the EMI filter. Here, the LISN is used as the input feed to replace the R_s matrix. These are also used to evaluate the full system to determine whether the system meets the specification.

LISN 常用在 EMI 测试实验室和不同的测试规范中（图 14.3）。如果测试规范要求使用一个 LISN，那么这就可以使用这个 LISN 矩阵来设计 EMI 滤波器。此处，LISN 还可做为馈入源使用并取代 R_s 矩阵。另外，LISN 也常常用来测试整个系统是否满足规范要求。

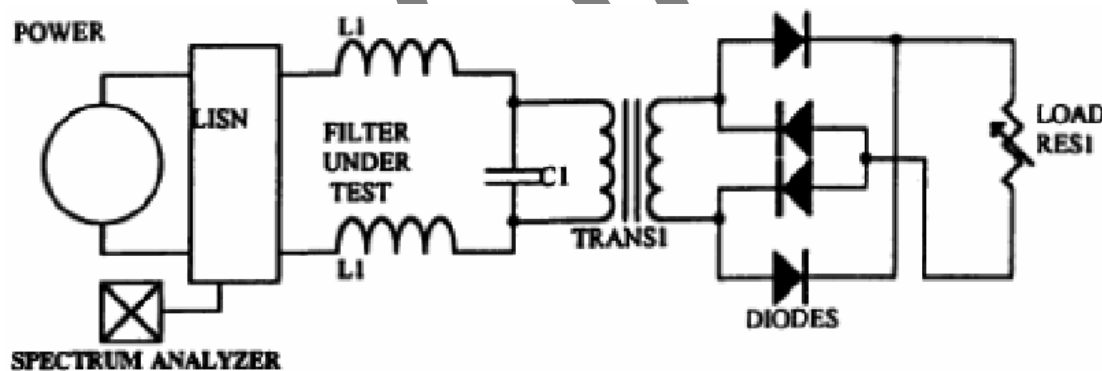


Figure 14.3 The LISN used for testing.

Standard LISN units (Figure 14.4) can be purchased from such companies as Solar Electronics Co. (Hollywood, CA 90038; Attn: Al Parker).

标准的 LISN (图 14.4) 可以向类似于 Solar Electronics(Hollywood, CA 90038; Attn: Al Parker)这类公司购买。

The LISN matrix is the most difficult to format and is formed by the following multiplication of the three matrices:

LISN 矩阵是最难计算的，它通过以下三个矩阵相乘得到：

$$\begin{bmatrix} 1 & 0 \\ \frac{R_1 + JX_{c1}}{R_1^2 + X_{c1}^2} & 1 \end{bmatrix} \begin{bmatrix} 1 & JX_{l1} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{R_2 + JX_{c2}}{R_2^2 + X_{c2}^2} & 1 \end{bmatrix} \quad (14.7)$$

Solving the first two,
先将头两个矩阵相乘, 得

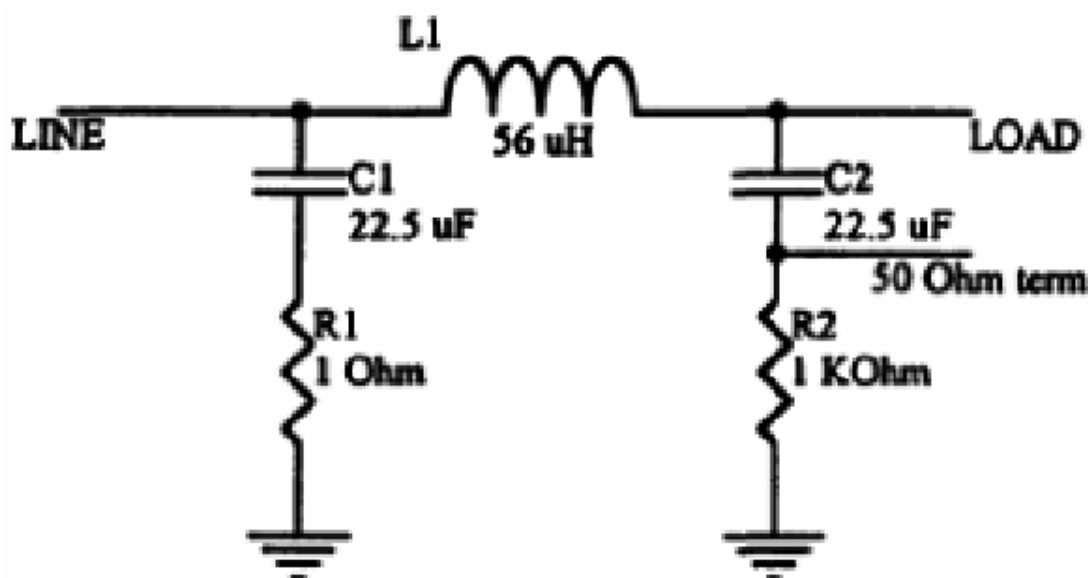


Figure 14.4 The common LISN.

$$\begin{bmatrix} 1 & JX_{l1} \\ \frac{R_1 + JX_{c1}}{R_1^2 + X_{c1}^2} & 1 + \frac{JX_{l1}(R_1 + JX_{c1})}{R_1^2 + X_{c1}^2} \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{R_2 + JX_{c2}}{R_2^2 + X_{c2}^2} & 1 \end{bmatrix} \quad (14.8)$$

The full solution is
全部相乘的结果是

$$\begin{bmatrix} 1 + JX_{l1} \frac{R_2 + JX_{c2}}{R_2^2 + X_{c2}^2} & JX_{l1} \\ \frac{R_1 + JX_{c1}}{R_1^2 + X_{c1}^2} + \frac{R_2 + JX_{c2}}{R_2^2 + X_{c2}^2} + \frac{JX_{l1}(R_1 + JX_{c1})(R_2 + JX_{c2})}{(R_1^2 + X_{c1}^2)(R_2^2 + X_{c2}^2)} & 1 + \frac{JX_{l1}(R_1 + JX_{c1})}{R_1^2 + X_{c1}^2} \end{bmatrix} \quad (14.8)$$

Typical LISN values with F_0 at 4000 are as follows:

Line section	Midsection	Load section
$R_1 = 1 \Omega$	$L_1 = 56 \mu H$	$R_2 = 50 \Omega$
$C_1 = 22.5 \mu F$		$C_2 = 22.5 \mu F$

$$X_{c1} = \frac{1}{2pKF_0C_1} = \frac{1.768}{K}$$

$$X_{L1} = 2pKF_0L_1 = 1.407K$$

$$X_{c2} = \frac{1}{2pKF_0C_2} = \frac{1.768}{K}$$

Using the standard outline of the 2×2 matrix with eight terms, the equations for the individual terms follow.

使用标准的 8 项 2×2 矩阵，表达式的各项如下

$$\begin{bmatrix} A + JB & C + JD \\ E + JF & G + JH \end{bmatrix}$$

The terms for the matrix with the preceding values simplified are as follows:
前述矩阵各项的简化值如下：

$$A = 1 - \frac{X_{L1}X_{Co}}{R_o^2 + X_{Co}^2} = 1 - \frac{1.407 \times 1.768}{50^2 + 1.768^2 / K^2} = 1 - \frac{1.407 \times 1.768 K^2}{50^2 K^2 + 1.768^2}$$

$$B = J \frac{R_o X_{L1}}{R_o^2 + X_{Co}^2} = J \frac{50 \times 1.407 K}{50^2 + 1.768^2 / K^2} = J \frac{50 \times 1.407 K^2}{50^2 K^2 + 1.768^2}$$

(14.10)

$$C = 0$$

$$D = JX_{L1} = J1.407K$$

$$E = \frac{R_i R_o (R_i + R_o) + R_i X_{Co}^2 + R_o X_{Ci}^2 - X_{Li} (X_{Co} R_o + R_i X_{Co})}{(R_i^2 + C_{Ci}^2)(R_o^2 + X_{Co}^2)}$$

X_{Co} is often the same as X_{c1} . This reduces the equation greatly to
 X_{Co} 常与 X_{c1} 相同，则上式可大大简化为：

$$\frac{(R_1 + R_2) + |R_1 R_2 + X_{C2}^2 - X_{L1} X_{C2}|}{(R_1^2 + X_{C2}^2)(R_2^2 + X_{C0}^2)}$$

where R_1 and R_{in} are the same, which also follows for C_1 and C_{in} . R_o (R_{out}) and C_o are equal to R_2 and C_2 . These values are interchangeable, as in the LISN shown in Figure 14.5.

此处 R_1 和 R_{in} 、 C_1 和 C_{in} 相同， R_o (R_{out}) 和 R_2 、 C_o 和 C_2 相同。在如图 14.5 所示的 LISN

中，这些值是可以互换的。

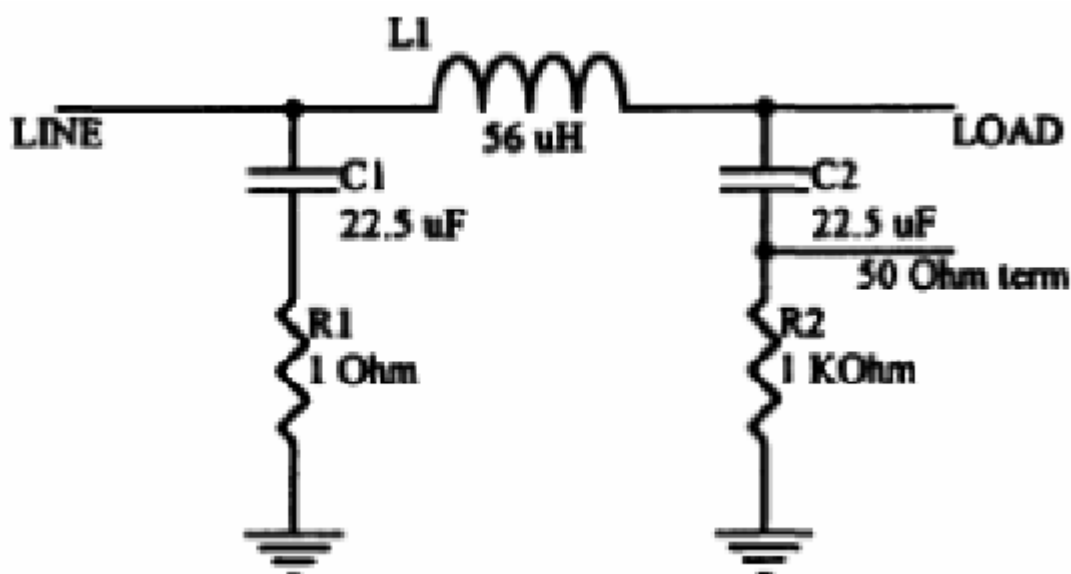


Figure 14.5 The common LISN with equal capacitors.

$$E = \frac{51K^2(47.51K^2 + 1.768^2)}{(K^2 + 1.768^2)(50^2 K^2 + 1.768^2)}$$

$$F = J \frac{X_{Ci}(R_o^2 + X_{Co}^2 - C_{L1}X_{Ci}) + X_{Co}(R_i^2 + X_{Ci}^2) + R_iR_oX_{L1}}{(R_i^2 + X_{Ci}^2)(R_o^2 + X_{Co}^2)}$$

X_{Co} is often the same as X_{Cin} . This greatly reduces the equation to
 X_{Co} 常与 X_{Cin} 相同，则上式可大大简化为：

$$F = J \frac{X_{Co}[R_o^2 + R_i^2 + X_{Co}(2X_{Co} - X_{L1})] + R_iR_oX_{L1}}{(R_i^2 + X_{Co}^2)(R_o^2 + X_{Co}^2)}$$

$$F = J \frac{[70.35K^5 + 4417.34K^3 + 11.053K]}{(K^2 + 3.126)(2500K^2 + 3.126)}$$

$$G = J \frac{R_i^2 - X_{L1}X_{Ci} + X_{Ci}^2}{R_i^2 + X_{Ci}^2}$$

$$G = \frac{3.126 - 1.488K^2}{K^2 + 3.126}$$

$$H = J \frac{R_i X_{L1}}{R_i^2 + X_{Ci}^2} = J \frac{1.407K^3}{K^2 + 3.126}$$

In the computer program, all these are already provided but the component values must be entered if these are different.

在软件中通常都提供了这些值，但是如果实际应用中它们与软件中的数值不同的话，那么就需要输入这些单元的值。

Finally, the component values (A-H) are entered based on the simpler equations 最后，要做的是输入这些基于简化方程得到的单元值 (A-H)。

$$P = 2pF_0 K$$

$$A = \frac{1 + P^2 R_2^2 C_2^2 - P_2 L_1 C_2}{1 + P^2 R_2^2 C_2^2}$$

$$J = \frac{P^3 C_o^2 L_1 R_o}{1 + P^2 C_o^2 R_o^2}$$

$$C = 0$$

$$D = JPL$$

$$E = P \frac{\{R_i C_i^2 [1 + P^2 C_o (R_o^2 - L)] + R_o C_o^2 [1 + P^2 C_i (R_i^2 - L)]\}}{(1 + P^2 C_i^2 R_i^2)(1 + P^2 C_o^2 R_o^2)}$$

$$F = JP \frac{C_i (1 + P^2 C_o^2 R_o^2) + C_o (1 + P^2 C_i^2 R_i^2) + P^2 C_i C_o L_1 (P^2 R_i R_o C_i C_o - 1)}{(1 + P^2 C_i^2 R_o^2)(1 + P^2 C_i^2 R_i^2)}$$

$$G = \frac{1 + P^2 C_{in} (C_{in} R_{in}^2 - L)}{1 + P^2 C_{in}^2 R_{in}^2}$$

$$H = J \frac{|P^3 C_1^2 R_1 L_1|}{(1 + P^2 C_1^2 R_1^2)}$$

The only variable is P, and this term varies with K. Again, this allows all these equations to be plotted as a function of K. K is the normalized frequency, which has the value of 1 at the cutoff frequency.

式中唯一的变量是 P ，它们项随 K 值变化。同样，可以作为 K 的函数绘出这些方程的曲线图。 K 是归一化频率，其在截止频率下值为 1。

§14.5 The DIN and DOUT Matrices

§14.5 DIN 和 DOUT 矩阵

A dissipative filter gives a loss of 6 dB per octave. The DIN faces the line and the DOUT faces the load if both filters are used. Several terms must be specified, including R_{in} and R_{out} . The value of K is the same as K in the other filters. R_{in} in Figure 14.6 (bottom) should be the desired filter input impedance, such as 50Ω for the DIN filter. R_1 , the output impedance needed, should match the load for the DOUT, which can also be 50Ω . This would be a nice feature for the 220A specification. Here, the term is R_{out} but R_4 is used in Figure 14.6 (bottom). The opposite two resistors, R_{out} (R_2 in Figure 14.6, bottom) for DIN and R_{in} (R_3 in Figure 14.6, bottom) for DOUT, can be used to match any filter wanted-Butterworth, π , or other-and these can also be, here, designed for 50Ω . 损耗型滤波器的插损为 6dB/倍频。如果使用两个滤波器，那么 DIN 面向电源线而 DOUT 面向负载。包括的 R_{in} 和 R_{out} 几项都需要指定值。此处的 K 值与其它类滤波器的 K 值相同。在图 14.6（底部电路）中的 R_{in} 应是预期的滤波器输入阻抗，如对于 DIN 滤波器为 50Ω 。需要的输出阻抗对于 DOUT 应与负载匹配，其值为 50Ω 。这对于 220A 规范来讲是一个非常好的优点。此处使用的是 R_{out} 但在图 14.6（底部电路）使用的是 R_4 。DIN 的 R_{out} （在图 14.6 底部表示的电路中的 R_2 ）和 DOUT R_{in} （在图 14.6 底部表示的电路中的 R_3 ）的可以用来匹配任何设计需要的巴特沃斯滤波器、 π ，或其它的滤波器，并且也可以在此处设为 50Ω 。

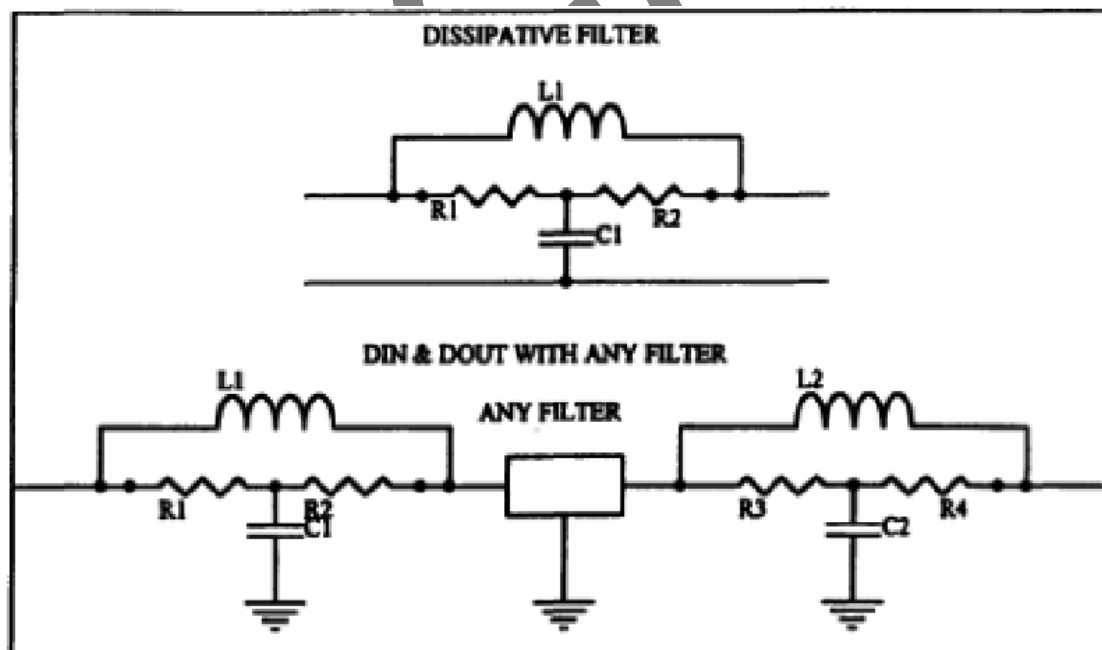


Figure 14.6 The DIN and DOUT.

The Δ is not always equal to 1 because of conversion back and forth between Y and A matrices. This leads to minor errors, or rounding errors, within the terms. The values of K and F_0 could come from the 'Common Term' area, and

the values of R_d , R_i , and R_o should be listed with this matrix. Both DIN and DOUT are the same, but R_i and R_o should switch values. As F_0 decreases in value, both L and C increase in value. If the line frequency is 400 Hz, the central filter cutoff should be 4000 Hz and above, say 4000 Hz. Then, if K_{ratio} is 0.5, or making its cutoff = 8000 Hz and still have the full filter give a good impedance match at 10,000 or 14,000 Hz, say 50Ω , the DIN and DOUT equations are

由于在 Y 和 A 矩阵之间反复变换, 所以导致 Δ 常常不等于 1。这会在各项中产生小误差。K 和 F_0 的值可以通过“共模项”得到, 而 R_d 、 R_i 和 R_o 则要和矩阵一起列出。DIN 和 DOUT 一般是相同的, 但对于不同的 R_i 和 R_o 就应相应地转换数值了。当 F_0 值下降时, L 和 C 的值都上升。如果电源线频率为 400Hz, 中心的滤波器截止频率应该为 4000Hz 或更高, 此处取 4000Hz。那么, 如果 K_{ratio} 为 0.5 或令其截止频率等于 8000Hz, 并还能使滤波器能在 10,000 或 14,000Hz 频率下达到阻抗匹配, 此处阻抗取 50Ω , 那么 DIN 和 DOUT 等式为

$$\begin{aligned} K_d &= K K_{ratio} & R_d &= \sqrt{R_{in} R_{out}} \\ L &= \frac{R_d K_{ratio}}{2\pi F_0} & C &= \frac{K_{ratio}}{2\pi F_0 R_d} \end{aligned} \quad (14.11)$$

where K_d is the equivalent of the value of K in the other filters, R_d is the design impedance for the DIN and DOUT only, and F_0 is the cutoff frequency for all the filters, including the DIN and DOUT.

此处 K_d 是在其它滤波器中 K 值的等效值, R_d 是 DIN 和 DOUT 的设计阻抗, 当然此值应是所有滤波器的设计阻抗包括 DIN 和 DOUT。

The format of the DIN or DOUT matrix is the same as the others:

DIN 或 DOUT 矩阵的形式与其它矩阵相同:

$$\begin{bmatrix} A + JB & C + JD \\ E + JF & G + JH \end{bmatrix} \quad (14.12)$$

If the design calls for all the R to be 50Ω , K_d is equal to 1, and $K_{ratio}=1$, the various elements A-H, equal the end values given after each element:

如果设计要求 R 为 50Ω , $K_d=1$, $K_{ratio}=1$, 那么不同的元 A-H 等于下式中对应每组的第二项值:

$$A = \frac{4K_d^2 R_d^2 - K_d^2 R_i (R_i + R_o) + (R_i + R_o)^2}{4K_d^2 R_d^2 + (R_i + R_o)^2}$$

$$A = 0.75$$

$$B = \frac{2JK_d^3 R_d R_i}{4K_d^2 R_d^2 + (R_i + R_o)^2}$$

$$B = J0.25$$

$$C = \frac{K_d^2 R_d^2 (R_i + R_o)}{4K_d^2 R_d^2 + (R_i + R_o)^2}$$

$$C = 12.5$$

$$D = \frac{J(2K_d^3 R_d^3 + K_d R_d (R_i + R_o))}{4K_d^2 R_d^2 + (R_i + R_o)^2}$$

$$D = J37.5$$

$$E = \frac{K_d^2 (R_i + R_o)}{4K_d^2 R_d^2 + (R_i + R_o)^2}$$

$$E = 0.005$$

$$F = \frac{J(2K_d^3 R_d^2 + K_d (R_i + R_o)^2)}{R_d (4K_d^2 R_d^2 + (R_i + R_o)^2)} \quad (14.13)$$

$$F = J0.015$$

$$G = \frac{4K_d^2 R_d^2 - K_d^2 R_o (R_i + R_o) + (R_i + R_o)^2}{4K_d^2 R_d^2 + (R_i + R_o)^2}$$

$$G = 0.75$$

$$H = \frac{2JK_d^3 R_d R_o}{4K_d^2 R_d^2 + (R_i + R_o)^2}$$

$$H = J0.25$$

Typical values are $F_0 = 4000$, $K_{ratio} = 1$, $R_i = 50$, and $R_o = 50$. Then, $K_d = K$, $R_i + R_o = 100$, and

典型值为 $F_0 = 4000$, $K_{ratio} = 1$, $R_i = 50$, $R_o = 50$ 。那么, $K_d = K$, $R_i + R_o = 100$ 和

$$\begin{bmatrix} 0.75 + j0.25 & 12.5 + j37.7 \\ 0.005 + j0.015 & 0.75 + j0.25 \end{bmatrix} \quad (14.14)$$

as shown by the preceding solutions of A-H. Note that the Δ is equal to 1. These are the values at 4000 Hz.

注意， Δ 等于 1，而且这些值是 4000Hz 频率下的值。

DIN and DOUT are the same, but R_i and R_o , if the two values are different, exchange values, so that the R_i of DIN faces the line and the R_o of DOUT faces the load. The K_{ratio} is usually 1 but must be the same if both DIN and DOUT are used. This means that two matrices are required, one for DIN and one for DOUT.

DIN 和 DOUT 是相同，但是对于 R_i 和 R_o ，如果两种值不同，就需要变换数值使 DIN 的 R_i 面对电源线，DOUT 的 R_o 面对负载。 K_{ratio} 常为 1，但是如果同时使用 DIN 和 DOUT 时 K_{ratio} 值是必须相同的。这意味着需要两个矩阵，一个用于 DIN 且另一个用于 DOUT。

§14.6 The RCSHU Matrix

§14.6 RCSHU 矩阵

The RCSHU matrix is used to lower the Q of the filter and correct for resonant rises and/or a problem frequency, such as insufficient loss at a given frequency. The design method is to calculate the needed capacitor value to equal the design impedance at the problem frequency and then place this combination in series across the line. These are normally mounted in board between two other filter sections, such as between two Ls, and would be tied across the first L's capacitor. This filter section can often cure several problems at once. If, for example, a three-stage L is needed to achieve the required insertion loss at 10 kHz, two resonant rises appear in the graph. As the load impedance deviates from the design impedance, the peak value of the resonant rise changes. Also, the loss near 10 kHz may be at, or even somewhat over, the insertion loss limit. Determine the lower resonant rise frequency, and tie the resultant network across either the first or the second L's capacitor. The result should be that the first resonant rise is reduced and the second resonant rise should be eliminated. The loss around 10 kHz, assuming that the first resonant rise is well below 10 kHz, is improved. Circuit Q is reduced to impede any oscillations by the addition of an RC shunt. (Figures 14.7 and 14.8). This is easier to design than the Cauer and is automatically balanced.

RCSHU 矩阵用在低 Q 值的滤波器中，它可以校正谐振增益问题和某个频率点下的问题，例如在一个给定的频率下插损不足的问题。设计方法是先计算出在谐振频率点下等于设计阻抗的电容值，然后将这个串联回路并于电源线间。通常这个电路常常位于滤波器其它部分电路的中间，例如在双 L 型滤波器条件下，安装在两个 L 型滤波器的连接处。通常这种滤波器可以同时解决几个问题。例如，如果需要三阶 L 型滤波器来满足 10kHz 频率点下的插损要求，则会在插损图中会出现两个谐振增益点。当负载阻抗偏离设计阻抗时，谐振增益的峰值会发生变化，此时在 10kHz 附近的插损可能会微微超过插损限值。具体解决方法是，确定较低的那个谐振增益频点，并将 RC 旁路连接在第一个或第二个 L 滤波器的电容

器处，结果是第一个谐振增益点降低了，并且第二个谐振增益点也被消除了，最终 10kHz 附近的损耗提高了（此处假设第一个谐振增益点远低于 10kHz）。通过 RC 傍路（图 14.7 和图 14.8），电路 Q 值降低到可以防止任何振荡。这种滤波器比考尔滤波器容易设计，而且其电路会自动平衡。

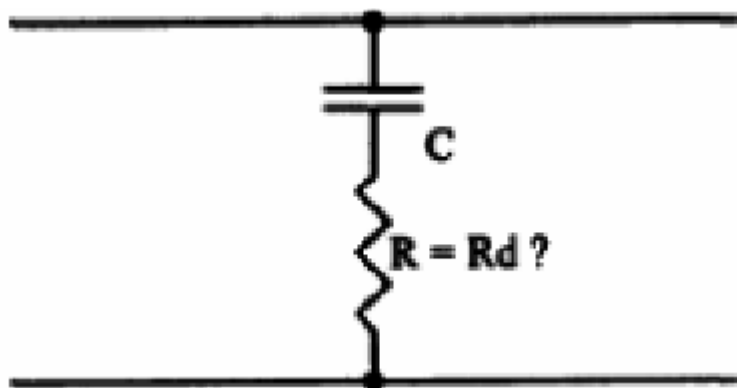


Figure 14.7 The RC shunt.

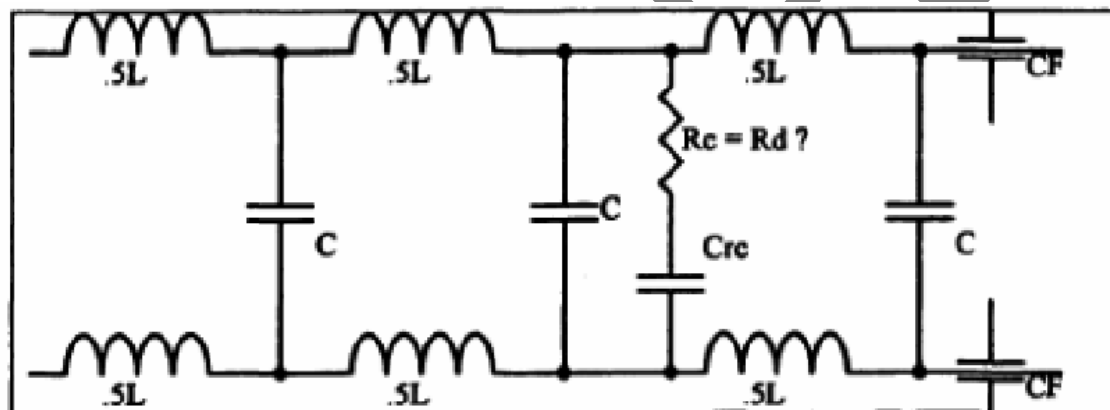


Figure 14.8 The multiple L with RC shunt.

The matrix is simple to form: R_c is the series resistance and should be equal to R_d , the design impedance from the ‘Common values to all filters,’ if any such area exists, or listed here. C is calculated as before, and $X_c = R_d$ at the problem frequency. The proper values are placed in the E+JF area of the matrix as listed here. Once the value of the capacitor is known, the capacitive reactance for the matrix must be a function of K , so the matrix varies with the frequency and can be plotted.

RC 傍路的矩阵也很容易组建： R_c 为串联阻抗其值应等于“所有滤波器都相同”的设计阻抗 R_d 。 C 按前面的方法计算，且在存在问题的频率点 $X_c = R_d$ 。如此处列出的那样，相应的值将会置于矩阵的 E+JF 区域。一旦电容值为已知，那么容抗矩阵将是 K 的函数，所有矩阵会随频率变化并可以绘出其曲线。

$$X_c = \frac{1}{2pF_0 KC} \quad (14.15)$$

$$E = \frac{R_c}{R_c^2 + X_c^2} \quad F = \frac{JX_c}{R_c^2 + X_c^2}$$

$$\begin{bmatrix} 1+J0 & 0+J0 \\ E+F & 1+J0 \end{bmatrix} \quad (14.16)$$

A triple L was designed with two resonant rises. The first fell near 3800 Hz and the second near 4600 Hz, and the design impedance was 10 Ω. This filter was also out of limits at 14 kHz. Design the capacitor impedance to equal the 10 Ω at 3800 for the first, lowest, resonant rise. This gives

例如一个三 L 型滤波器有两个谐振增益点，第一个在 3800Hz 附近而第二个点在 4600Hz 附近，并且其设计阻抗为 10 Ω。同样这个滤波器也会在 14kHz 超过限值。具体的设计是，第一步先在较低的谐振增益频率点 3800Hz 处使电容阻抗等于 10 Ω。这样就得到

$$C = \frac{1}{2\pi \cdot 3800 \times 10} = 4.188mF = 4.2mF$$

The self-resonant frequency (SRF) of this capacitor need not be as good as that of the rest of the filter capacitor unless there are also higher frequency problems. This is primarily used to solve some low-frequency problems, and the highest frequency is 14 kHz in the example just stated. If the SRF(原文为 SFR, 译者注) is better than the fifth harmonic, 70 kHz here, of this upper frequency, the job will get done. This statement is made so that the filter designer does not select a capacitor that costs many times more than the capacitor that will do the job. Note that X_c is a function of K , not a single value as shown earlier. Tie the 10 Ω resistor and the 4.2 uF in series across one of the inbound capacitors that make up the first or second L counting from the load end of the filter. The closer to the load, the better this network works, and the load is the higher impedance.

除非在较高频率下也有噪声问题，否则此电容的自谐振频率不需要与其它滤波器电容一样好。这个电容只是用来解决较低频率的问题。如果此例中问题出现的最高频率为 14kHz，并且如果它的自谐振频率高于这个上限频率的 5 次谐波，此处是 70kHz，那么这个电容就能发挥其性能。以上这些论述就是为了避免滤波器设计者错误选用比实际能满足要求的电容器成本高许多倍的电容器。注意到 X_c 是 K 的函数，而不是早前我们使用的单一值。将 10 Ω 电阻与 4.2uF 电容串联，并将这个电路并在从负载端开始数的第一个或第二个滤波器的电容上。当负载是高阻抗时，这个电路离负载越近，其效能愈佳。

§14.7 The Series Inductor LSER and the Shunt Capacitor CSHU

§14.7 串联电感 LSER 和傍路电容 CSHU

These matrices should be understood from the various descriptions given earlier but are reviewed again here for clarity. There are many uses for each of these, and in some locations they can be used together. For example, these two together can make up L_s , T_s , π_s , and so forth that are not functions of R_d , CSHU,

alone, can be used to duplicate the value of a feedthrough capacitor. The LSER, the series inductor, can be a common mode inductor. LSER and CSHU can work together to form part of the common mode filter (Figure 14.9).

现在我们通过前面的各种矩阵论述，现在应很清楚本节的矩阵了，但此处为明确一下会再次回顾前面的论述。通常本节的这些矩阵中的每个矩阵都常常会用到，有时也会一起使用。例如，这两类矩阵组合后就会形成 L、T、 π 和其它多级滤波器，通常这些矩阵并不只是 R_d 和 CSHU 的函数。另外电容也可以使用同值的穿心电容来代替，而串联电感 LSER 也可以是共模电感。这样 LSER 和 CSHU 就可以组合为共模滤波器的一部分（图 14.9）。

The LSER is

$$X_l = 2pF_0KL \quad (14.17)$$

It is obvious that the value of X_l is a function of K and is placed in the matrix at D:

显然 X_l 的值是 K 的函数，并置于矩阵的 D 项：

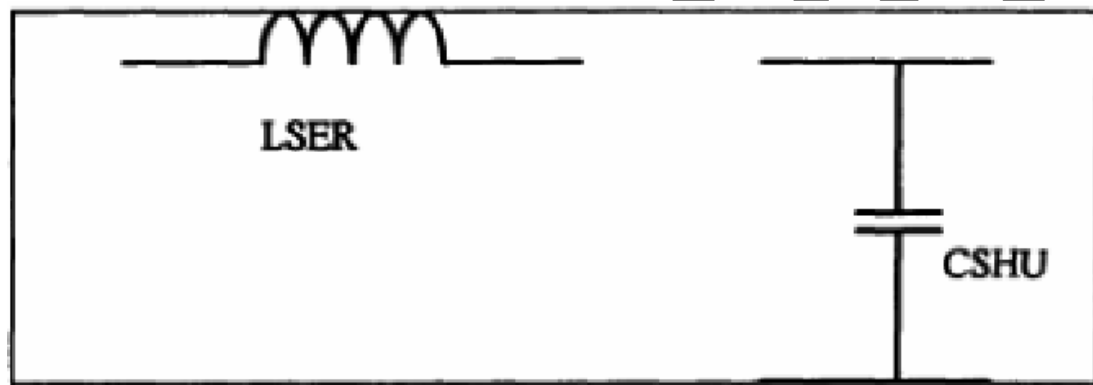


Figure 14.9 The LSER and CSHU.

$$\begin{bmatrix} 1 + J0 & 0 + JX_l \\ 0 + J0 & 1 + J0 \end{bmatrix} \quad (14.18)$$

The CSHU is

$$X_c = \frac{1}{2pF_0KC} \quad (14.19)$$

This is the same as RCSHU except that R_c is zero, making the E value zero and F the reciprocal of X_c :

这里除了 R_c 为零外，其它都类似于 RCSHU，令 E 值为零，且 F 在 X_c 的倒数项内，则

$$X_c = \frac{1}{2pF_0KC} \quad (14.20)$$

§14.8 The L Martrix

§14.8 L 矩阵

This is a review of Section 11.2 showing the origin of the values that make up the L filter, where K is the normalized frequency and R_d is the design impedance (Figure 14.10).

这部分是对 11.2 节的回顾，给出的是组成 L 型滤波器的初始值。此处 K 是归一化频率， R_d 是设计阻抗（图 14.10）。

$$F = KF_0$$

$$L = \frac{R_d}{2\pi F_0}$$

$$X_l = \frac{2\pi F R_d}{2\pi F_0} = KR_d$$

$$C = \frac{1}{2\pi F_0 R_d}$$

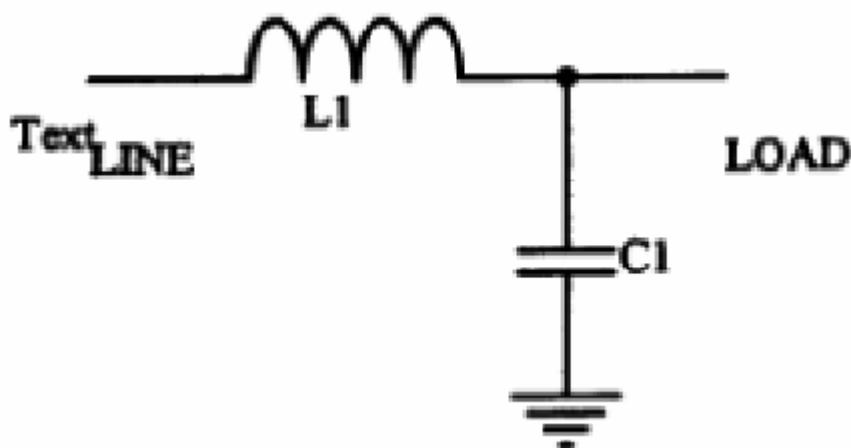


Figure 14.10 The single L filter.

$$X_c = \frac{2\pi F_0 R_d}{2\pi F} = \frac{R_d}{K}$$

Here, the inductors and capacitors are treated as pure. The series element of inductive reactance is placed in the JD term, and the reciprocal of this impedance of the shunt capacitor is placed in the JF term. The inductor faces the line, and the capacitor faces the load. The L matrix is formed as follows:

此处，电感和电容按理想元件处理。其感抗置于 JD 项，旁路电容的阻抗的倒数项置于 JF 项。在电路结构次序上，电感面向电源线，电容面向负载。则 L 型滤波器的矩阵形式如下：

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} 1+J0 & 0+JKR_d \\ 0+J0 & 1+J0 \end{bmatrix} \begin{bmatrix} 1+J0 & 0+J0 \\ 0+\frac{JK}{R_d} & 1+J0 \end{bmatrix} \begin{bmatrix} V_{out} \\ I_{out} \end{bmatrix} \quad (14.21)$$

Eliminate the unnecessary zero here only because the eight positions must be filled so that the computer program reads the full eight units. This way the same solution can be reused repeatedly, like a template.

将没用的零去掉（前面写成 8 项而没把零去掉是因为计算机程序的数据读取需要 8 项的形式，这种方法如同使用模板一样，可以重复使用相同的数据）。

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} 1 & JKR_d \\ J0 & 1 \end{bmatrix} \begin{bmatrix} 1 & J0 \\ \frac{JK}{R_d} & 1 \end{bmatrix} \begin{bmatrix} V_{out} \\ I_{out} \end{bmatrix} \quad (14.22)$$

The new matrix becomes

新矩阵变成

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} 1-K^2 & JKR_d \\ \frac{JK}{R_d} & 1 \end{bmatrix} \begin{bmatrix} V_{out} \\ I_{out} \end{bmatrix} \quad (14.23)$$

Then, inserting the other zeros so that the L has the same form as the rest, 然后，再插入零项（凑 8 个项的位置—译者注），这样 L 型滤波器矩阵就与其它矩阵形式一致了。

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} 1-K^2+J0 & 0+JKR_d \\ 0+\frac{JK}{R_d} & 1+J0 \end{bmatrix} \begin{bmatrix} V_{out} \\ I_{out} \end{bmatrix} \quad (14.24)$$

§14.9 The π Matrix

§14.9 π 矩阵

In the π filter (Figures 14.11 and 14.12), the capacitor value is split. Half is placed in front of the inductor in parallel with the line, and the other half is in parallel with the load. The capacitive reactance of both halves is then doubled. Yet, the reciprocal of this impedance placed in term JF or half the value is then used to make up the L matrix in term JF.

在 π 型滤波器中（图 14.11 和 14.12），电容值是拆分開的。一半置于电感前且并在线间，令一半并在负载端。这样这两个半值电容的容抗就被加倍了。此时可以将此加倍后的容抗的倒数置于 JF 项。另外在构建 L 矩阵时，JF 项需取整个电容容抗值的倒数。

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} \frac{1}{JK} & 0 \\ \frac{1}{2R_d} & 1 \end{bmatrix} \begin{bmatrix} 1 & JKR_d \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \frac{1}{JK} & 0 \\ \frac{1}{2R_d} & 1 \end{bmatrix} \begin{bmatrix} V_{out} \\ I_{out} \end{bmatrix} \quad (14.25)$$

The π matrix is the same form as the others.

π 矩阵与其它矩阵的形式相同。

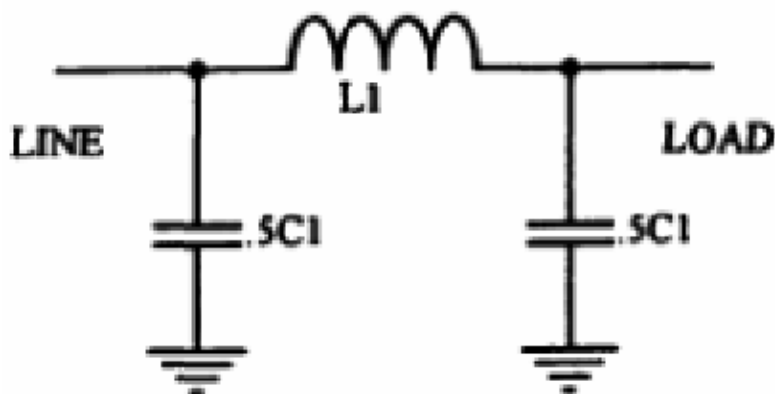


Figure 14.11 The π filter.

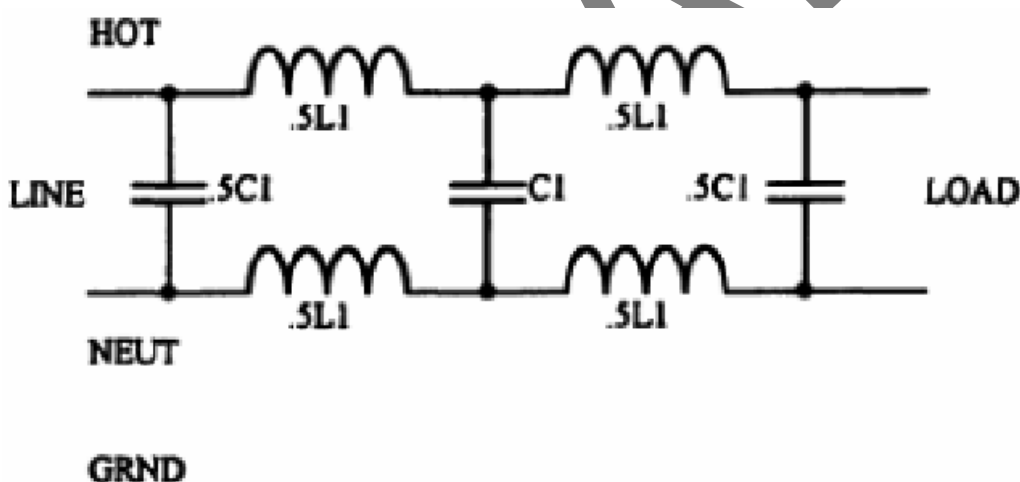


Figure 14.12 The multiple balanced π filter.

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} 1 - \frac{K^2}{2} + J0 & 0 + JKR_d \\ 0 + \frac{JK(4 - K^2)}{4R_d} & 1 - \frac{K^2}{2} \end{bmatrix} \begin{bmatrix} V_{out} \\ I_{out} \end{bmatrix} \quad (14.26)$$

§14.10 The T Matrix

§14.10 T 矩阵

In the T filter (Figures 14.13 and 14.14), the inductor is split, with half of the inductor in series with the line and the other half in series with the load. This

makes the JD term half the value of the π or L. The full T matrix is

在 T 矩阵中电感值是拆分的。一半串于电源线端，另一半串在负载端。这使得 JD 项只是 π 和 L 矩阵的半值。整个 T 矩阵为

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} 1 & \frac{JKR_d}{2} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{JK}{R_d} & 1 \end{bmatrix} \begin{bmatrix} 1 & \frac{JKR_d}{2} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_{out} \\ I_{out} \end{bmatrix} \quad (14.27)$$

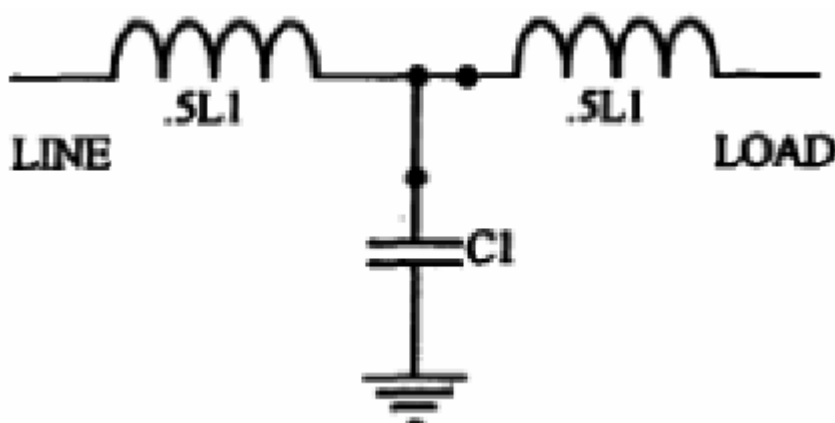


Figure 14.13 The T filter.

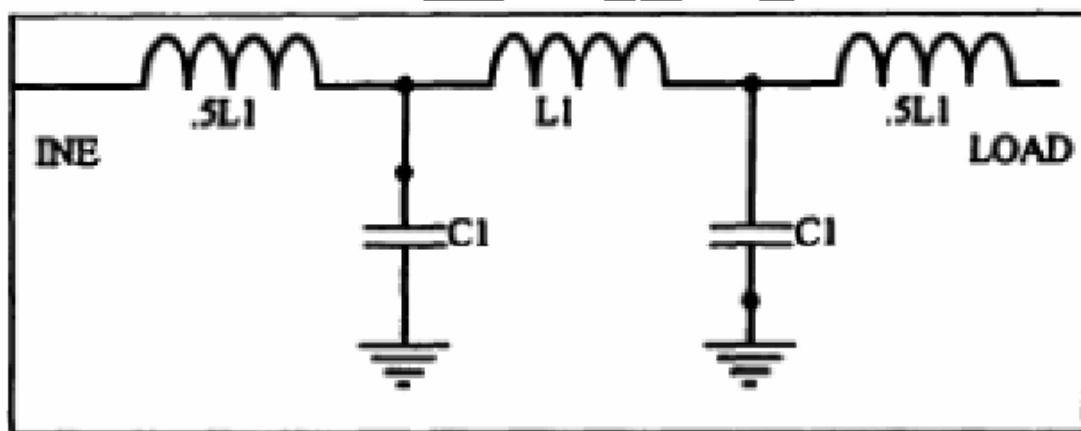


Figure 14.14 The multiple T.

which becomes

变为

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} 1 - \frac{K^2}{2} + J0 & 0 + \frac{JKR_d}{2} \left(2 - \frac{K^2}{2} \right) \\ 0 + \frac{JK}{R_d} & 1 - \frac{K^2}{2} + J0 \end{bmatrix} \begin{bmatrix} V_{out} \\ I_{out} \end{bmatrix} \quad (14.28a)$$

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} \frac{(2-K^2)}{2} + J0 & 0 + \frac{JKR_d(4-K^2)}{4} \\ 0 + \frac{JK}{R_d} & \frac{2-K^2}{2} + J0 \end{bmatrix} \begin{bmatrix} V_{out} \\ I_{out} \end{bmatrix} \quad (14.28b)$$

§ 14.11 The Cauer Matrix or Elliptical Filter

§ 14.11 Cauer 矩阵或椭圆滤波器

The Cauer filter (Figure 14.15) is used to eliminate a problem frequency. In the 461 specifications in which 100 dB or so is needed at 10-14 kHz, a Cauer filter is sometimes used. F_m is the problem frequency, and R_c is the resistance in series with the cap. Above F_m , the Cauer looks like a capacitor and the resistor limits the minimum impedance in this capacitor leg. The impedance of R_c is usually assigned the value of R_d , the design impedance of the filter. This is usually employed on the center inductor of a triple-L network. The Cauer is often associated with a triple-L filter (Figure 14.16). The inductor value is the same as before:

考尔滤波器（图 14.15）是用来消除某个问题频率点的。在 461 规范中在 10~14kHz 频率范围下需要 100dB 插损时，有时就会使用到考尔滤波器。 F_m 是问题频率点， R_c 是串联在电容后的电阻。在频率 F_m 之上，考尔滤波器看上去像是一个电容并且串联的那个电阻会限制电容引线的最小阻抗。阻抗 R_c 通常设计为滤波器设计阻抗 R_d 。考尔滤波器常并联在三 L 型滤波器网络中心的电感上。考尔滤波器常与三 L 型滤波器结合使用（图 14.16）。其中的电感值与前面的相同：

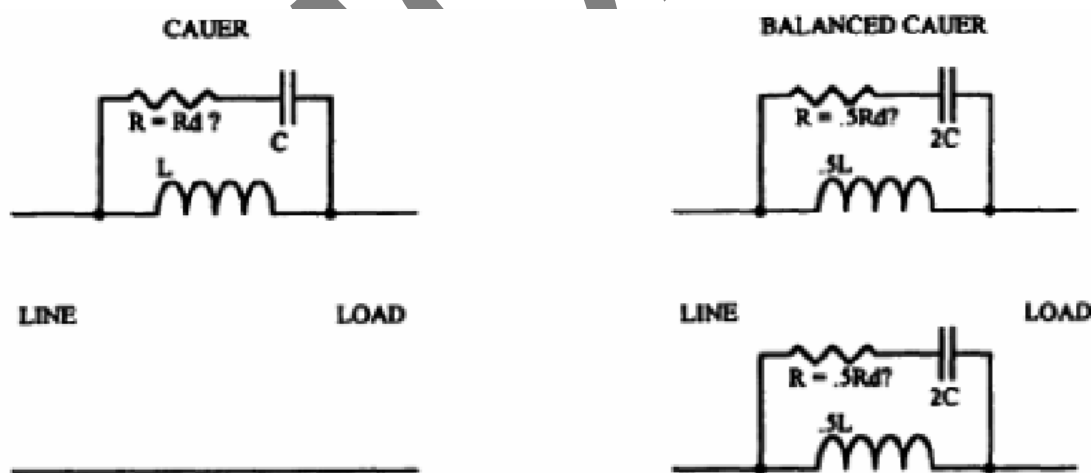


Figure 14.15 The Cauer matrix.

$$L = \frac{R_d}{2pF_0} \quad (14.29)$$

and the Cauer capacitor must resonate with L at the problem frequency F_m .

且 Cauer 滤波器电容必须在问题频率点 F_m 与 L 谐振。

$$C = \frac{F_0}{2pF_m^2 R_d}$$

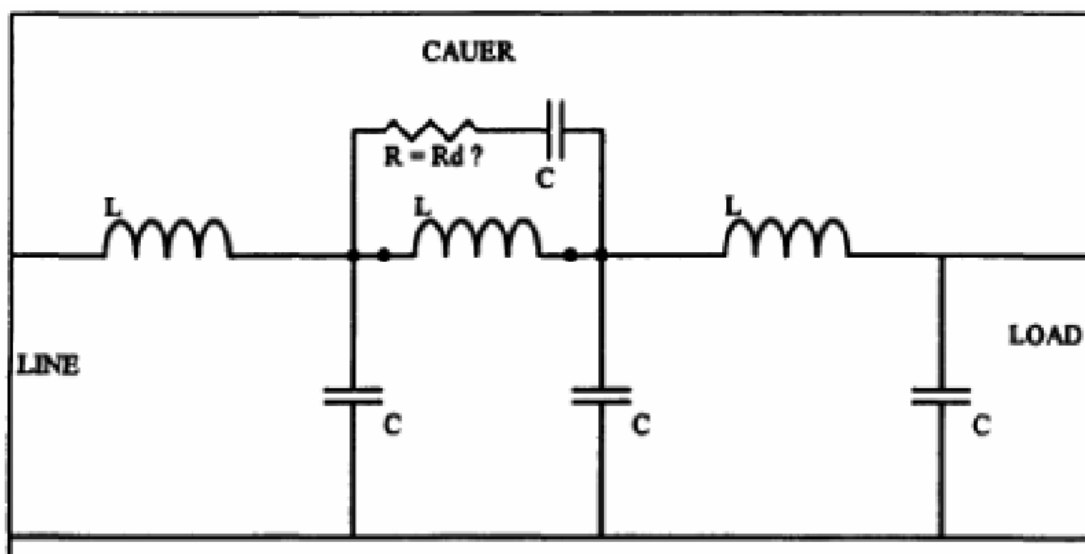


Figure 14.16 The Cauer of elliptical filter.

The impedances are

阻抗是

$$X_l = KR_d \quad X_c = \frac{2pF_m^2 R_d}{2pF_0 F} = \frac{M^2 R_d}{K} \quad (14.30)$$

where M is the multiplier to convert from F_0 to F_m :

此处 M 为从 F_0 转换为 F_m 的乘数：

$$F_m = MF_0$$

$$C = \frac{K^4 R_c R_d^2}{K^2 R_c^2 + R_d^2 (K^2 - M^2)}$$

and

$$D = J \frac{(K^3 R_c^2 R_d^2 - K^3 M^2 R_d^3 + KM^4 R_d^3)}{K^2 R_c^2 + R_d^2 (K^2 - M^2)}$$

R_c and R_d should be equal but here are listed separately if for any reason they should be different for a special problem an engineer may encounter. If the two terms are equal, C and D reduce to

式中的 R_c 和 R_d 应相等，但此处分别列出，以便于工程师面临特殊问题时可以使用不同值。如果这两项相等，C 和 D 简化为

$$C = \frac{K^4 R_d}{K^2 + (K^2 - M^2)} \quad (14.31a)$$

which approaches R_d at the higher K values, and
此式在较高 K 值时近似等于 R_d ，且

$$D = J \frac{(K^3 R_d - K^3 M^2 R_d + K M^4 R_d)}{K^2 R_c^2 + R_d^2 (K^2 - M^2)} \quad (14.31b)$$

This approaches
近似为

$$D = -J \frac{R_d M^2}{K}$$

which is the capacitive reactance, and this approaches zero as the frequency increase.

此式为容抗，当频率增加时其值接近于零。

The matrix for the Cauer filter is
考尔滤波器的矩阵为

$$\begin{bmatrix} 1 + J0 & C + JD \\ 0 + J0 & 1 + J0 \end{bmatrix} \quad (14.32)$$

and without the zeros is
去掉零项变为

$$\begin{bmatrix} 1 & C + JD \\ 0 & 1 \end{bmatrix}$$

15

Matrix Applications

矩阵应用

The first step is to find the filter type needed for application. The listing in Section 5.8 should help. Either through documentation from the electromagnetic interference (EMI) test house or mathematically from Chapter 10, the required insertion loss must be known. This is often given as a list of frequencies and the required loss at each. The filter must be checked at each frequency to make sure the loss is met at each frequency. The load current, input voltage, and line frequency must be known to obtain the design impedance R_d and find the minimum cutoff frequency. Calculate the value of R_d by dividing the voltage by the expected highest load current, and the cutoff frequency should be 10 times the line frequency.

应用矩阵的第一步是要确定滤波器类型。5.8 节的列表会对此有帮助。不论是 EMI 测试室的文件还是第 10 章的数学计算都需要知道滤波器的插入损耗。这种插损需求常常以列表形式给出：不同频率点对应要求达到的插损。通常这就需要在每个频率点检测滤波器，以确保滤波器能满足插损要求。另外，负载电流、输入电压和电源线频率也需要给出，这样就可以计算出设计阻抗 R_d 和最小截止频率。一般将电压除以预期的最高负载电流就可以计算出 R_d 的值了，并且截止频率应为电源线频率的 10 倍。

The first matrix in the chain, or cascade, should be a matrix that represents the line. This could be the R_s , LINESIM, LISN, or any other line unit added by the user. These are not part of the filter. The second, third, fourth, and so on, are parts of the filter. These are matrices multiplied together, and the final matrix is solved for the full loss of the filter. As K varies the loss changes, and this can be plotted.

在这个矩阵链中的第一个矩阵应是一个表示电源线的矩阵。这个矩阵可能为 R_s 、LINESIM、LISN 或使用者增加的其它单元，当然它并不是滤波器的一部分。第二、三、四...个矩阵分别为滤波器的各个部分。这些矩阵乘在一起得到的最终矩阵就是此滤波器的整体损耗。当 K 变化时插入损耗也随之变化，同样这可以画出图表来表示。

One condition discussed here is the low-current application in which operational amperes is used. Many design engineers make errors when using this application. These engineers substitute active filters to replace passive components in the lower current applications. These filters must have very *clean power* or they cross talk, generating the same noise, and in some cases even more noise, than this active filter was meant to cure.

此处讨论的应用一个条件就是低电流，在此类应用条件下许多设计者常会弄错。在低电流

应用条件下,有些工程师常用有源滤波器来替代无源滤波器,但是这些有源滤波器必须需使用纯净的电源,否则就会发生串扰并产生和有源滤波器想要清除的噪声相同的噪声,甚至会产生更大的噪声。

§ The single -Phase AC Filter

§ 单相 AC 滤波器

For example, an L is chosen by the filter designer. The design impedance is found to be 10Ω , and the line frequency is 400 Hz. The loss needed is 40 dB at 20 kHz. This is a low frequency, and the R_s matrix is chosen for the first matrix to represent the line. R_s is thought to be around 4Ω at 20 kHz. The second matrix is the L matrix chosen by the engineer. If these are automatically multiplied as a system in the computer, all the other matrices in the chain contain unit matrices. The final matrix is the result of only the R_s and the L filter because only they control the answer. The value of F_0 is changed to meet this 40 dB loss by varying the value of F_0 or by using a program like GOAL-SEEKER (a shareware program). In the newest Lotus program, this feature is built in. The engineer should add 6 dB for headroom to the loss. This gives the filter designer some latitude on component values without fear of harming the performance of the filter. This also gives some additional attenuation to an unknown frequency spike that could push the equipment when using the filter over the limit. The value of F_0 here is 1200 Hz to obtain the desired loss of 46 dB (40+6 headroom), and this is sitting on the third harmonic, may too low. Another L filter is added. Skip by one matrix, and leave it as a unit matrix. This allows changing it later to an RCSHU, or whatever, if needed. To review:

例如,滤波器设计者选择了 L 型电路,且设计阻抗需要 10Ω ,电源线频率为 400Hz,并且在 20kHz 频率下插损要求为 40dB,可见这个频率是很低的。现在选择第一个矩阵来表示电源线,其源阻抗 R_s 在 20kHz 时约为 4Ω 。第二个矩阵为 L 矩阵。如果软件上的矩阵链都作为一个系统在计算机内自动相乘,那么矩阵链中其它所有的矩阵都需要取值为单元矩阵(只有第一和第二矩阵取实际值)。这样最终的结果就只有 R_s 和 L 滤波器矩阵了,当然这是因为实际上只有这两个矩阵影响最终结果。设计上可以通过改变 F_0 值来满足 40dB 的插损要求,也可以使用像 GOAL-SEEKER (一个共享软件) 这样的软件来计算。在最早的 Lotus 软件中,都内建有这种特性。另外设计工程师还需要为插损增加 6dB 的余量,这样滤波器设计者就可以使用具有一定范围的元件值,而不必害怕元件值的某些变化会损害滤波器的性能。这种增加余量的方法同样也会对未知频率下的尖峰有额外的衰减,如果不增加余量则有可能使得设备在未知尖峰的作用下超过限值。此处为得到 46dB (40+6 余量) 的损耗, F_0 值应选为 1200Hz,这个频率点正处在三次谐波频点上,或许还有些低了。如再加另一个滤波器,则跳过一个矩阵并将其保留为单元矩阵。这个预留的单元矩阵可以在需要时更换成 RCSHU 或其它什么需要的矩阵。现在回顾一下:

Matrix 1: R_s

Matrix 2: L

Matrix 3: unit

Matrix 4: change to L

All remaining matrices (所有保留矩阵) : units

This is followed by the column matrix with elements V_o and I_o , as shown in Chapter 14. I_o can be replaced by V_o/R_d , where R_d is the design impedance and is the lowest load resistance seen by the filter. Proceed by adding the next L filter. This changes the cutoff frequency to 4600 Hz, which is well above the 4000 Hz recommended limit. The initial inductance was 1.3 mH, and now the requirement is two filter at 345 uH. The same is true for the capacitor. It was 13.3 uF and is now two at 3.46 uF. This can be balanced as in Figure 15.1. The load impedance was changed to see how the filter responded in the standby mode, and a resonant rise was found at 2760 Hz. This required an RCSHU to be added to the third matrix; add the common mode components to Figure 15.2. The new matrix lay out is as follows:

这个矩阵链接下来是由 V_o 和 I_o 组成的列矩阵（如第 14 章所表示的列矩阵）。其中 I_o 可以用 V_o/R_d 来代替。此处 R_d 为设计阻抗并且是从滤波器看过去的最低负载阻抗。接下来会再加下一个 L 型滤波器，此时会将截止频率改变为 4600Hz，可以看到此截止频率明显高于 4000Hz 的推荐频率限制。最初的电感为 1.3mH，但现在的要求则是两个滤波器电感均为 345uH，同样电容初始为 13.3uF 而现在两个滤波器都为 3.46uF。此电路可以像图 15.1 那样采用平衡电路结构。负载阻抗的改变要视滤波器在等待模式下如何响应而定，且谐振增益为 2760Hz。这就需要一个 RCSHU 加在第三个矩阵上（原来空出的单元矩阵—译者注），并以后会进一步增加共模元件（见图 15.2）。此时新的矩阵链如下：

Matrix 1: R_s

Matrix 2: L

Matrix 3: now an RCSHU

Matrix 4: L

All remaining matrices: units

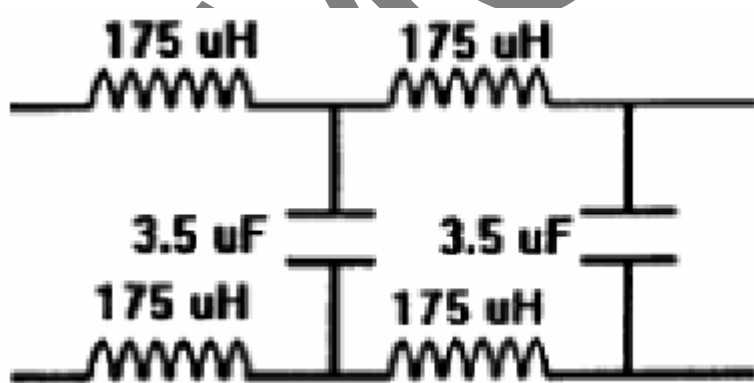


Figure 15.1 The balanced L.

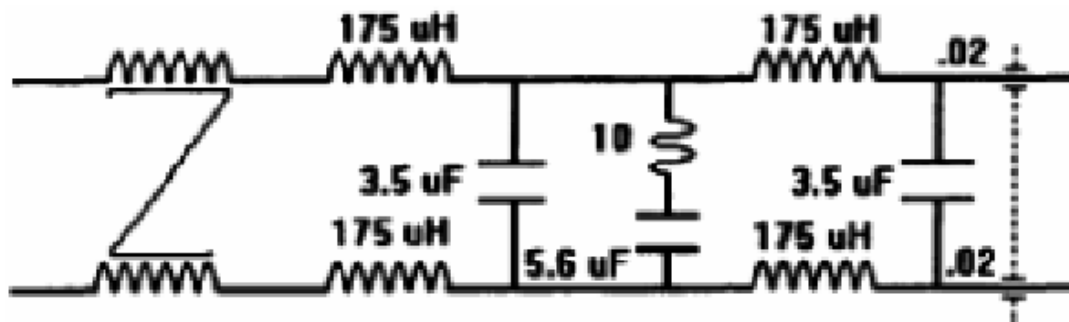


Figure 15.2 The fully balanced double L with Zorro, RCSHU, and feedthroughs.

This matrix group is still followed by the column matrix with elements V_o and V_o/R_d . Check that all dB losses at the other frequencies listed in the specification meet their requirements for this filter. Most expect all the losses at the higher frequencies pass if the lowest passes. This is usually true but there are exceptions, so that all losses must be checked. This topic is treated later, but in general the frequency that requires the lowest cutoff frequency determines the cutoff frequency uses.

在这个矩阵群后仍然是以 V_o 和 V_o/R_d 为矩阵元的列矩阵。接下来，检查规格书中要求满足的所有的频率点的 dB 损耗。一般会预期：如果最低频率的插损通过了，那么较高频率条件下也会全部通过。事实上也常常是如此的，但也会有例外，所以还是需要检测所有的插损。这方面的话题会在稍后讨论，一般情况下应用中需要的最低截止频率率决定截止频率的选取。

The remaining job is to determine the Z (Zorro). The two feedthrough capacitors are added, giving 0.04 uF (Figure 15.3). The line-to-line capacitors are out of the circuit, along with the RCSHU. The 175 uH inductors are divided by 2, giving 87.5, a total of only 175 uH for the four, adding little to the common mode insertion loss. Yield all this to headroom. This is reduced to a single L.

目前剩下的工作就是确定 Z (Zorro)。如图 15.3 增加的两个穿心电容的总容值为 0.04uF。将线间电容和 RCSHU 从电路中去掉，175uH 的电感器一分为二，每个 87.5uH，其实对于四电感的总值为 175uH 对共模损耗几乎没有什么影响。还有，对这些值都要考虑余量。现在这个电路简化为单 L 电路。

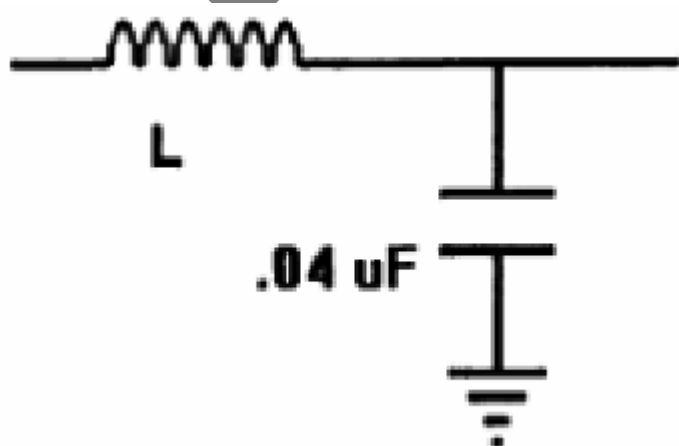


Figure 15.3 The common mode part of the filter in Figure 15.2.

Remove or replace these elements with the unit matrix, except the R_s and matrix 2, which is an L. The loss for the common mode is 46 dB at the switcher frequency of 50 kHz. The 0.04 μF capacitor must be maintained. This requires an impedance of 1125 Ω and a cutoff frequency of 3550 Hz. The Zorro is 50.4 mH, which is ridiculous. The filter was designed to component level, but the Zorro should be fixed. Some would substitute any reasonable lower value, hope for the best, and pray for an exemption from the specification, if the unit fails. The circuit is shown in Figure 15.4.

除了 R_s 矩阵和矩阵 2 (L 型矩阵), 将前面矩阵链中那些矩阵都用单元矩阵来代替。在开关频率为 50kHz 的频率下, 其共模损耗为 46dB。当然必须保留 0.04 μF , 这就需要阻抗为 1125 Ω 并且截止频率为 2550Hz。另外对于 Zorro 为 50.4mH, 显然这个数值大得荒谬可笑。虽然滤波器要设计成使用标准值的元件, 但是对于 Zorro 却是需要符合实际需求值的。一些人会用低值来代替高值, 并希望可行, 而当滤波器测试没有通过时就会恳求规格书降低要求。最后的电路如图 15.4 表示。

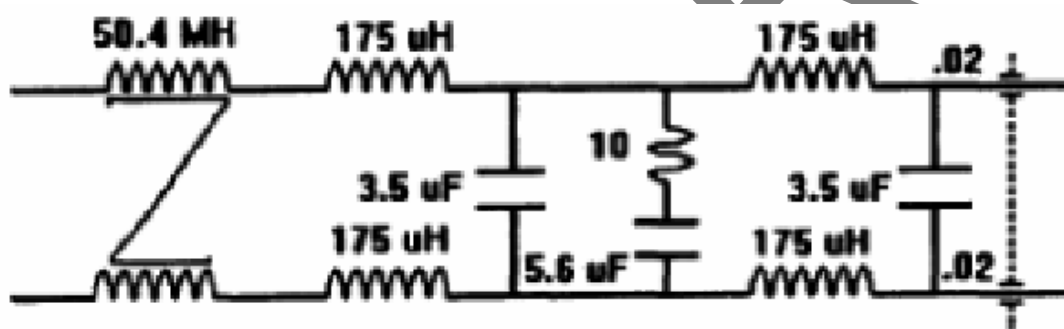


Figure 15.4 The value of Zorro for Figure 15.1

All that remains is to design the two different inductors and capacitors or choose a supplier. This filter may be out slightly when tested but should require only minor changes at best. High-frequency problems? Add Capcon (see Chapter 4) or ferrite beads. Differential problems at the switcher? Improve the quality of the RCHU capacitor, or increase its value and/or raise the inductors to 180 μH , or 200 if needed. Common mode? Increase the Zorro somewhat. Too high a value for the common mode inductor, as earlier? Change the feedthrough values to 0.01, and add a second section. This is now a double L, as in Figure 15.5.

所有剩下的工作就是设计这两类不同的电感和电容并选择供应商。实际测试时, 此滤波器一般只会有轻微不符合的情况, 因此设计方案只需做很小的修改。不符合的情况如果是高频的问题, 那么增加 capcon (见第四章) 电容或磁珠即可; 如果是开关电源产生的差模问题, 提高 RCHU 电容质量或增加电容值和/或同时把电感值增加到 180 μH , 甚至在需要时增加到 200 μH ; 对于共模问题, 则要稍微增加 Zorro 的值; 对前面遇到的共模电容量太高的问题, 则可以将穿心电容改为 0.01 μF , 并再增加第二节滤波器。这时电路就是双 L 型, 如图 15.5 所示。

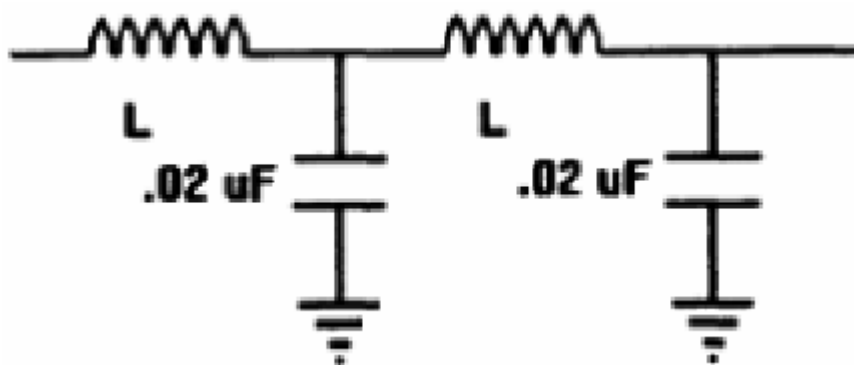


Figure 15.5 The calculation of the double Zorro.

The new value of each Zorro is 7.9 mH. Now, the case could still be presented again by examining the contribution of the differential mode to the common mode filter. One set of parallel differential inductors aids each common mode inductor. The parallel value of these inductors is 87.5 uH. The Zorro is still an order of magnitude greater than the 87.5 uH and is still not subtracted to lower the size of the Zorro. This difference is left to increase the headroom. Note that this filter (Figure 15.6) has an internal shield to ground (the case). Note also how the size of the Zorro has dropped. This is also a much more designable inductor with this much current.

新的 Zorro 值就变成了 7.9mH。因为要考察差模电路对共模的贡献，现在需要重新表述一下这个例子。如一套互相平行的差模电感都加上共模电感，其中这对互相平行的电感的容量为 87.5uH。现在 Zorro 值仍然在量级上大于 87.5uH，而且目前还没为减少体积而降低 Zorro 的值。这个差模量增加了共模的余量。注意最终的滤波器（图 15.6）有一个内部的对地屏蔽层（壳）。还应注意，Zorro 的尺寸是如何下降的。当然在大电流条件下，这还是可以进行设计的。

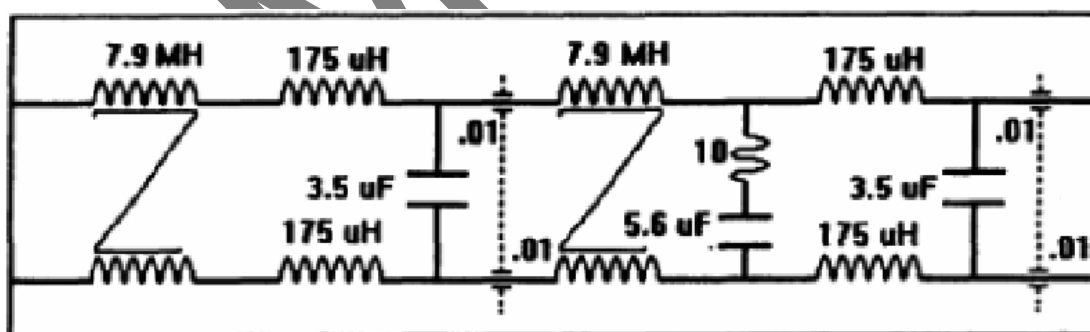


Figure 15.6 The balanced single-phase filter with two double-L common mode sections.

§15.2 The Three-Phase Filter

§15.2 三相滤波器

There are two types of three-phase filters. The first is the Y filter, and the second is the Δ filter. These two types are then divided into two groups. The first is the higher current type in which each leg is a separate insert, with each insert the

same type and size. This is very important because of the possibility of installing a smaller, neutral filter in any of the main legs.

三相滤波器有两种类型，第一种是 Y 型滤波器，第二种是△型滤波器。这两种滤波器又会分成两个类。第一类是大电流类型，每个引线分开插入同样类型和尺寸的电路。工程上这种设计方法是很重要的，因为这样就可以将小的零线滤波器安装到每相主电源线路上了。

Also, the third, sixth, ninth, and so on, currents add in-phase on the neutral wire along with the unbalanced current of the three legs. This harmonic content would be the odd multiples of 3 and a few of the even multiples, such as 6, 12, and so on. Therefore, the wire size and filter size are the same for the neutral as required for the other three legs.

同样，如果三相不平衡时，3、6、9 等次谐波电流按位相在零线上叠加。通常谐波量会是 3 的齐次倍数而很少为如 6，12 等偶数倍数。因此，对于零线的线径和滤波器尺寸与其它三相的要求是完全相同的。

$$\begin{aligned} & A \sin(\omega N t + N x_0) \\ & A \sin(\omega N t + N x_{120}) \\ & A \sin(\omega N t + N x_{200}) \\ & 3 A \sin(\omega N t) \end{aligned} \quad (15.1)$$

This assumes all the peak harmonic current on all three legs in the same. If not, the term 3A is replaced by A+B+C. The three phases add for all multiples of 3, if this harmonic exists. The sixth should be a very low level, if it exists at all, but the ninth is strong, especially when the off-line regulator is used as part of the power supply. Beware: multiphase transformers reduce these harmonics. This is a function of the number of phases used, but most designers eliminate the lower harmonics, such as the third harmonic. This eliminates the problem. The following approximate equation for the off-line regulator current is normalized to 1. Refer to Equation (3.1b):

上式假设三相所有的谐波峰值都相同，如果不同，3A 就会变成 A+B+C。如果谐波存在，那么所有 3 的倍数的谐波会三相相加，一般如果 6 次谐波存在的话谐波量也会较低，但 9 次谐波值则会较高，尤其是供电电源含有离线调节器时的情况。注意：多相变压器会降低谐波值，它是一个与使用相数相关的函数。一般多数设计者只考虑消除较低次的谐波，如 3 次谐波，这样就会解决问题。接下来的近似方程是按离线调节器电流归一化为 1 得到的。参考方程 (3.1b)：

$$\frac{4tT}{p} \sum_{N=1,3,5,7}^{\infty} \frac{1}{(T^2 - N^2 t^2)} \cos \frac{pNt}{2T} \sin \frac{pN}{2} \sin \frac{2pNt}{T} \quad (15.2)$$

If the 3, 9, 15, 21, and 27 are added, the peak almost reaches 0.7. This current, plus the unbalanced current, should prove that the neutral filter must be the same size as the other three legs. The last three-phase type is the lower current mode.

如果 3、9、15、21 和 27 次谐波相加，那么峰值会接近 0.7。这个电流会增加不平衡电流，这就要求零线滤波器必须和其它相滤波器尺寸相同。第二类三相滤波器的类型是低电流类。

To design the three-phase filter, the voltage and current seen by each filter leg must be known. Find the maximum power required by the load. Divide this by 3, and this is the power per leg. Divide this answer by the line-to-ground voltage for a Y filter or a line-to-line voltage for a Δ filter. Multiply, for the Δ filter only, the last answer by the square root of 3:

设计三相滤波器时，必须知道从每个滤波器引脚看过去的电压和电流值。通常找到负载的最低功率需求，并将之除以 3，结果就是每相所需的功率。对于 Y 型滤波器，需将这个结果除以线地电压；对于 Δ 型滤波器则除以线间电压，并对除出来的结果乘以根号 3。

$$\frac{12,000}{3} = 4000 \quad \frac{4000}{208} = 19.231 \quad (15.4)$$

$$19.231\sqrt{3} = 33.309 \quad 33.309\sqrt{2} = 47.106 \quad (15.5)$$

(此处出现公式编码错误，阅读时请注意，译者注)

If the total load power, taking all the inefficiencies into consideration, is 12 kVA, the power supplied by each line is 4 kVA. If the line-to-line voltage is 208 V, the current is 19.231 times the square root of 3. This equals 33.309 line A. Assuming that no off-line regulators are used, the current peak is 47.106 A. The inductors must not saturate at this current (here, 47.1 A). The design impedance is 208 V divided by 33.309, giving 6.24Ω . Use 6Ω for the design impedance.

如果将所有的无功功率也考虑在内，全部负载功率为 12kVA，每一相为 4kVA。如果线间电压为 208V，则电流为 19.231 的根号 3 倍，那么相电流就等于 33.309A。如果没有使用离线调节器，并假设此时电流峰值为 47.106A，那么就要求电感在 47.106A 电流偏置条件下不饱和。设计阻抗为 208V 除以 33.309，得 6.24Ω 。则可以取设计阻抗为 6Ω 。

§ 15.2.1 The Low-Current Y Filter

§ 15.2.1 低电流 Y 型滤波器

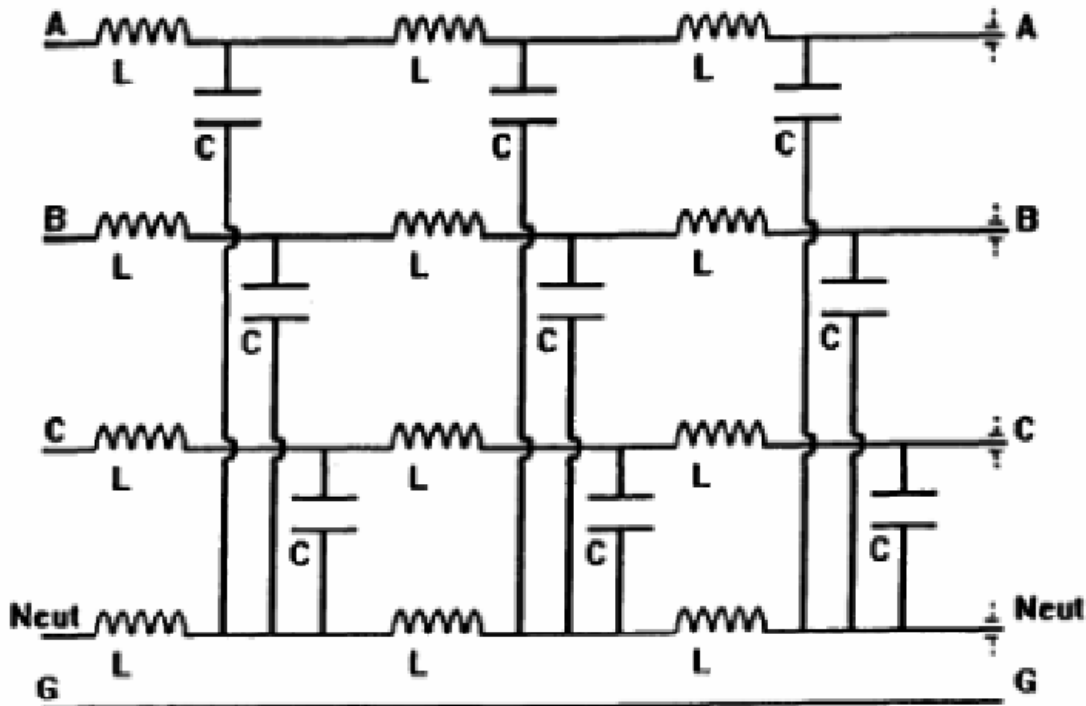


Figure 15.7 The low current Y 5 wire triple-L filter.

The power is from each leg to neutral, and the neutral current is zero if the currents of the three legs are well balanced (Figure 15.7). As mentioned earlier, however, the odd third-order harmonics are still present. This is true only for the fundamental of the power line frequency, as discussed earlier. In the low-current filter, all the components are in the same container and the capacitors are wired from the leg to neutral. This makes for smaller capacitors because of the change from 208 to 120 V, saving money, weight, and volume. 如果三相平衡，则零线电流为零（图 15.7）。然而如早先提到的，3 次的奇数倍谐波却仍存在。在低电流滤波器中，所有元件都放置在相同容器中，且电容连接在线地间。因为线地间电压为 120V 而不是相电压 208V，这样电容的容量就会比较小，因而会节省成本、重量和体积。

Y filters are often called five wire because of the three legs plus the neutral and the ground. The ground must be left intact and unfiltered. I have seen many filters from various filter manufacturers with components in the ground leg. This is a violation of the electrical code. The ground lead must be intact, not broken. 因为三相加零线和地线共 5 线，所以 Y 型滤波器常称为 5 线滤波器。注意，地线常需要保持完整且不能有滤波。我曾见过许多滤波器制造商在地线接元件的情况，这是违反电气原则的。地线必须保持完整而不能间断。

The only exception is if ferrite beads or toroids are slipped over the wire, leaving the ground lead in a solid wire.

只有一种情况例外，这就是如果磁珠或磁环套在线上，此时地线是实体的线并未发生中断。

The output feedthrough capacitors in Figure 15.7 are case to ground, and the ground wire is wired to the case. Also, this filter can use the Zorro common mode inductor for common mode rejection because all the parts are within the same enclosure.

图 15.7 中的输出穿心电容是通过壳接地，那么地线就需要和壳连接。同样可以使用 Zorro 共模电感来消除共模噪声，这是因为此低电流滤波器是所有的相线都在同一个壳体中的。

The common mode inductor cancellation of the magnetic field of the differential mode power current works as shown in Figure 15.8. Discussing the balanced fundamental power frequency first and ignoring the harmonics, the A, B, and C currents generate magnetic fields that cancel. Here, a magnetic field cannot be generated without current flow in the neutral common mode leg. If the system is unbalanced (we know that it is), the difference current flows in the neutral leg of the common mode inductor and still returns the common mode to balance. As far as the harmonics are concerned, whatever harmonic current flows in any leg also flows in the neutral leg and still cancels. Thus, as far as the power delivered to the load is concerned, the magnetic field of the common mode is neutralized. Any common mode pulse or signal, from either the load or the line, is attenuated by upsetting this balance. The design technique is the same. R_d is the lowest line voltage divided by the highest line current required by the equipment-not the inrush. Find the cutoff frequency, and the values of the inductors and capacitors follow.

共模电感中差模状态的工作电流的磁场是相互抵消的，如图 15.8。首先我们只讨论平稳的电源线频率而忽略谐波，那么 A、B 和 C 相电流的磁场相互抵消。此处磁场零线中没有电流就不会产生磁场。如果系统不平衡，那么零线中流过共模电感的差模电流同样会令共模电感出现平衡状态。现在考虑谐波的情况，无论每相谐波电流是多少，此谐波电流同样会流过零线进而使磁场相互抵消。因此，只要是功率向负载传输的情况，共模电感中的磁场都是相互中和的。但是对于任何从负载或电源线发出的共模噪声或信号，都会减弱这种平衡。三相的设计方法与单相是相同的，是最低线电压除以设备所需的最高电流（但不是涌入的电流）。接下来计算出截止频率、电容和电感值。

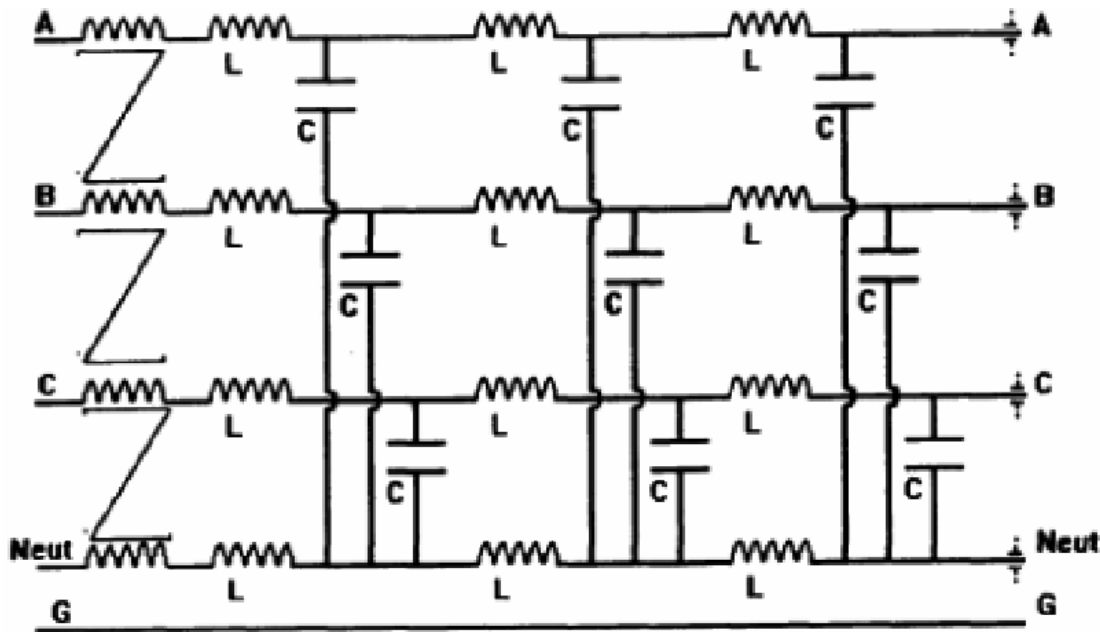


Figure 15.8 The low current Y 5 wire triple-L filter with Zorro.

§ 15.2.2 High-Current Y Filter

§ 15.2.2 大电流 Y 型滤波器

These become so large and heavy that they must be built using the insert technique. All three legs and the neutral are the same electrically and physically, and all inserts are installed in a larger enclosure. This way, if any leg bolts, only the failed filter of that leg must be replaced. This technique also eases installation by allowing the outer enclosure to be installed and then placing the inserts in this enclosure one at a time. This is better than hoisting the entire enclosure and contents, which has been done by various contractors. They installed all the inserts and hoisted the fully weighted unit and then dropped it. The entire filter had to be replaced at a premium cost because of time constraints. This was expensive, to say the least.

大电流 Y 型滤波器会又大又重，所以必须使用各相线分别插入滤波模块的方法来解决这个问题。对于三相和零线滤波模块具有相同的电路和物理结构，并安装在一个更大的滤波器壳体内。通过这种设计方法，滤波器可以在某一路出现故障时只更换故障模块。而且这种设计方法也允许使用统一的外部安装壳体，再在壳体内部分别安装各路模块，这样安装起来会比较简便。这种设计方法比许多制造商所采取的将所有元件都装在一个壳体内的方法要好些。更换整个滤波器会因为时间原因增加额外成本，至少这还是很昂贵的。

All the capacitors in Figure 15.9 are to ground. There are no components from line to line in this arrangement, such as capacitors or MOVs. The leakage specification, even with power factor correction coils, is rarely met. There really should not be a leakage current specification for this high-current type of filter. This should be known before the specification is written and often is not known or heeded by some specification writers. It has been requested after the filter is shipped that some leakage specification also be met that was not provided to

the manufacturer initially.

注意，图 15.9 中所有电容都是对地电容。在此电路没有如线间电容或线间 MOV 等线间元件。对于漏电流规范，即使带功率因数校正线圈也还不能达到要求。实际上对此类高电流滤波器不应采用漏电流规范。这一点规范制定者在书写规范之前就应了解，但实际上却常常不被留意。

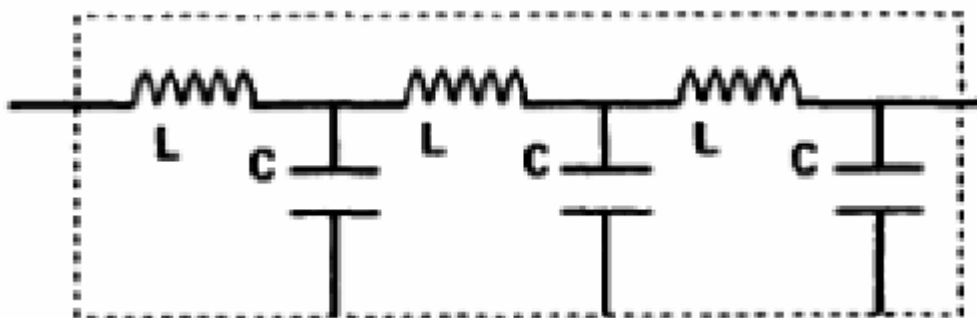


Figure 15.9 The single high-current insert.

There is some limited common mode in the differential inductors, which are in parallel, and the capacitors, which are also in parallel. Each inductor is divided by the number in parallel, and the capacitors multiply in parallel. Also, this assembly lacks the ability to use the Zorro common mode inductor for common mode rejection. In the following example, the equivalent circuit is composed of $L/4$ and $4C$, as shown in Figure 15.10.

在差模电感相互平行排列和电容相互平行排列时，在差模电感中会有一些有限的共模电感。对于并行排列的电感，每个的值应为原值除以平行的个数；对于并行排列的电容，则需要乘以并联的个数。当然这些累积的共模电感并没有 Zorro 共模电感那种抗共模噪声的能力。在下面的例子中，如图 15.10 所示，等效电路由 $L/4$ 和 $4C$ 组成。

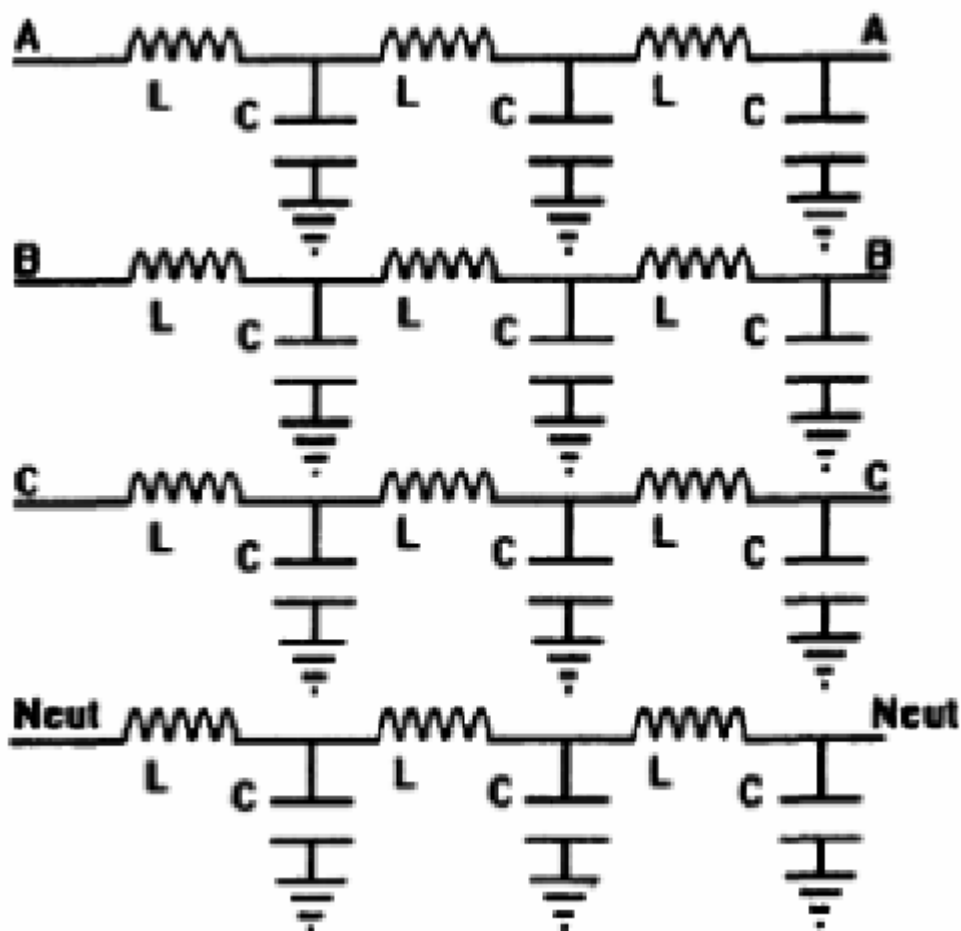


Figure 15.10 The three-phase four-wire filter.

The common mode equivalent is as shown in Figure 15.11. The working impedance is now one-fourth the design impedance, but the cutoff frequency is the same.

共模等效电路见图 15.11。现在工作阻抗是设计阻抗的 1/4，但是截止频率相同。

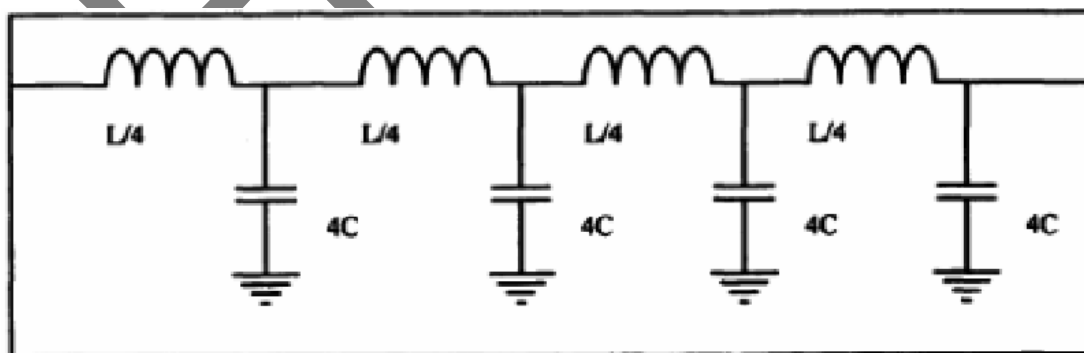


Figure 15.11 The common mode portion of the four-wire filter.

$$R_d = \sqrt{\frac{L/4}{4C}} = \sqrt{\frac{L}{16C}} = \frac{1}{4} \sqrt{\frac{L}{C}} \quad (L/4 \text{ 原文误为 } L4) \quad (15.6)$$

$$F_0 = \frac{1}{2p \sqrt{\frac{L}{4} 4C}} = \frac{1}{2p \sqrt{LC}} \quad (\text{原文误为 } L4/4C) \quad (15.7)$$

Follow the single-phase design method. R_d is the line voltage divided by the maximum line current in any one leg.

按单相设计方法， R_d 是电压除以最大每线电流。

§ 15.2.3 The Low-Current Δ

§ 15.2.3 低电流 Δ 型滤波器

This lower current type is often specified to pass 220A with the stipulation "to test any one line with the other two legs grounded." This is a good spot for the π type because the line and load impedances are both 50Ω . The line-to-line capacitors can be shared, giving twice the capacitance to ground (Figure 15.12). This makes our job easier.

这种低电流类滤波器是为通过 220A 规范而设计的，220A 规定“测试任何一线时都需要其它两线接地”。因为电源线和负载的阻抗按规定为 50Ω ，所以 π 型滤波器测试结果会很好。按 220A 的测试方法，线间电容可以共享，使得对地电容增加一倍（图 15.12）。这就使得我们的设计工作比较容易了。

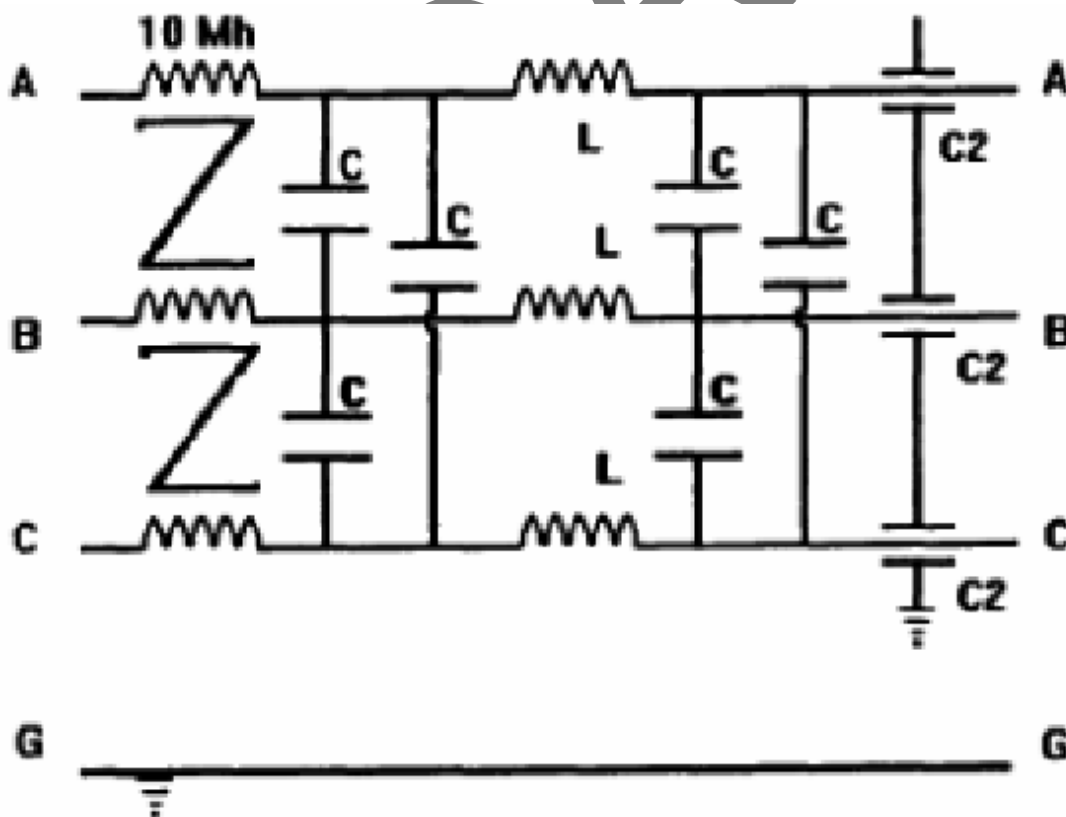


Figure 15.12 The four-wire Δ showing case ground for feedthrough operation.

If the A leg is under test in the 220A system, then legs B and C are grounded.

The capacitors from A to B and A to C are then in parallel on both sides of the differential filter inductor. The impedance is determined the same way using the line-to-line voltage and current. Follow the same procedure for the single phase. If the 220A specification is all that must be met, the capacitor values can be divided by 2, enabling smaller capacitors and saving money, weight, and volume. Choose the R_s for matrix 1, and place the π in matrix 2; the rest should be unit matrices.

如果在 220A 系统中测试 A 线，那么 B 和 C 需要接地，此时滤波器两端的 A-B 和 A-C 的电容就并联在一起了。同样，也此滤波器也采用与单相相同的方法通过线间电压和电流来计算阻抗。如果需要满足 220 规范，则电容容量可以减半，通过使用小容量电容可以节省滤波器的成本、重量和体积。软件中的矩阵链需做如下处理：矩阵 1 选 R_s ，矩阵 2 置 π 矩阵值，其余的矩阵置为单位矩阵。

Matrix 1: R_s

Matrix 2: π

Matrix 3: unit

Matrix 4: second π if needed

All remaining matrices: units matrices

Remember, this is followed by the column matrix. If the single π meets all the requirements, the design is finished. If not, add a second π for matrix 4, leaving matrix 3 a unit matrix. This is done for the same reason—to be able to add another network for matrix 3. Once the capacitor value is established, split the value between the lines. If the π is a multiple, check for a resonant rise and fix as before. Continue with the design as in the single phase. Check that each frequency listed in the specification meets the required loss of the list. If not, the filter may have to be redesigned for more loss or any of the other solutions depending on the frequency of the problem.

注意，此矩阵链后还要跟列矩阵。如果单 π 型滤波器满足所有要求，那么设计就结束了。如果没有满足，就在矩阵 4 中加入第 4 个矩阵，令矩阵 3 为单位矩阵。这么做是基于同样的原因——能在矩阵 3 中加入另一个电路网络。一旦电容值计算出来时，就将线间电容量取半（因为 220A 规范其它两线接地的原因—译者注）。如果是多 π 型滤波器，那么还需要检查谐振增益点并按前面的方法处理这些点。接下来的设计工作与单相相同，检查每个频率点规定的插损要求。如果不满足要求，就需要重新设计更大损耗的滤波器或采取基于问题频率点的其它解决方案。

§ 15.2.4 The High-Current Δ

§ 15.2.4 大电流 Δ 型滤波器

This is the same as the high-current Y except that the capacitors are again to ground. These should be from leg to leg, as in the low-current Δ . There is no convenient way to do this using the insert method. The value of the required capacitance should be doubled to return half the required reactance to ground and half to the other leg.

除了高电流 Y 型滤波器的对地电容之外，此类滤波器与 Y 型高电流滤波器基本相同。这些电容要像低电流 Δ 型滤波器那样接在线间。这样就不能使用各相线分立模块的方法了。

当然需要的电容值应加倍，这样对地和对其它相线的电抗就会减半。

§ 15.3 The DC-to-DC Filter

§ 15.3 DC-DC 滤波器

The dc-to-dc type is often the tubular type and is unbalanced. Figure 15.13 shows the proper hardware to install the tubular through a wall or equipment housing. Figure 15.14 shows the unit installed. The filter is often a single feedthrough capacitor, giving only 6 dB per octave loss. In some other filters, inductor(s) are included, making up the L or T type. These last two give 12 or 18 dB per octave. The filter requires a good ground, or the filter is out of business. If this is an L or T, then only the inductor(s) is in the circuit. This reduces the loss to 6 dB rather than the 12 or 18 dB that the L or T would give. What if the filter is a single feedthrough type? This would net zero loss, all because the filter is not grounded.

DC-to-DC 型常是管状的和非平衡电路的类型。图 15.13 显示的是在机壳上较好的安装方法。图 15.14 显示的是已安装好的滤波器。此类滤波器常由单穿心电容构成，其插损为 6dB/倍频。其它电路种类的滤波器中，还常使用电感做成 L 型和 T 型电路，其插损为 12 或 18dB 每倍频。此类滤波器需要良好接地，否则就会影响性能。如果接地不好则 L 型或 T 型电路就只有一个电感，那么插损也会减小到 6dB/倍频而不是 L 或 T 所具有的 12 或 18dB 每倍频。如果不良接地的是单穿心电容型会如何呢？结果是 0 插损，这都是因为滤波器没有接地导致电容不工作。

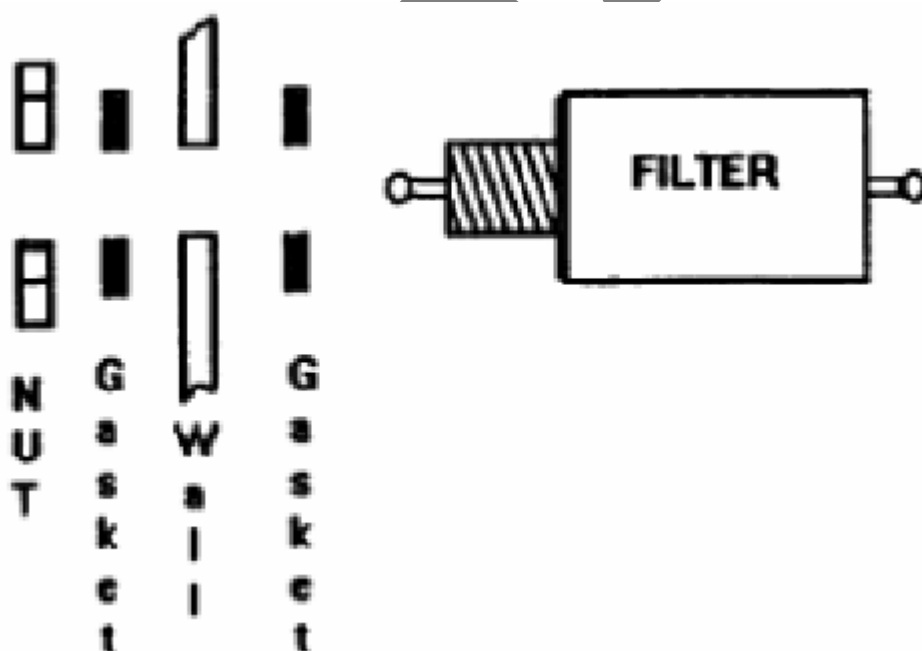


Figure 15.13 The unbalanced feedthrough filter.

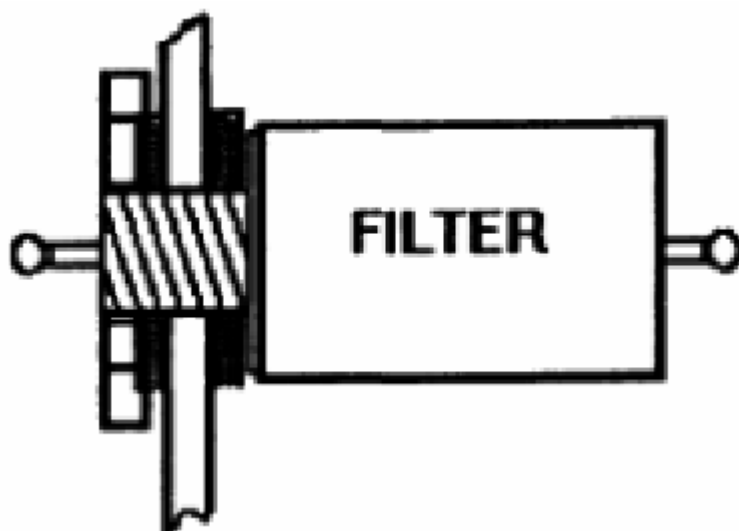


Figure 15.14 The installed feedthrough filter.

The construction is as follows (Figure 15.15). The output pin is a snug fit through the capacitor center arbor, and this pin is isolated from the outer wall. The capacitor is soldered to this outer wall washer (ground). The inductor and capacitor are soldered to the output pin. The outer tube is placed over the inductor and capacitor and soldered to the end plate. The inductor is soldered to the input pin pressed through the threaded area and extends into the I_d of the inductor. This top capacitor and threads are soldered to the tube, completing the unit.

此滤波器的结构如下 (图 15.15)。输出管脚是穿过电容中心轴的滑动针, 并且此针与外壁绝缘。电容焊接在外壁垫圈上 (地), 电容和电感焊接在输出管脚上, 滤波器外管覆盖了电容和电感并最终焊接在终端平面上。电感在穿线区焊接在输入管脚上, 并通过压力增加电感导通电流 I_d 。上部的电容和引线焊接在管子上形成一个整体。



Figure 15.15 The construction of the single-phase feedthrough.

§15.4 Low-Current Filters

§15.4 低电流滤波器

The low-current filter suffers from the opposite conditions that affect the high-current filter. Here, the inductances increase while the capacitor size decreases. One method is to employ RC filters in which the value of R should be

less than 10% of the minimum load resistance. The disadvantage is that the circuit gives only 6 dB per octave. A better method for low-current filters is to employ active filters (Figure 15.16). They are small and light and can be designed with many poles, but sometimes the higher frequencies suffer because of the open-loop gain of the operational amplifiers. What is often overlooked here is that the direct current feeding the operational amplifiers must be very clean. Therefore, the filter(s) needs a filter (Figure 15.17). There have been cases in which a number of high-impedance lines must be filtered. The plus and minus voltage for each operational amplifier must be filtered with an RC filter or a conventional passive filter, with the capacitor facing the load. The combined voltage feed must be filtered with a passive filter.

低电流滤波器面对的是与高电流滤波器相反的使用条件。此处，当电容尺寸减小时电感需增加。一个解决办法是使用 RC 滤波器，其中 R 应小于最小负载阻抗的 10%。这种方法的缺点是只有 6dB/倍频的插损。另一个较好的低电流滤波器设计方法是使用有源滤波器（图 15.16）。它们很轻巧，并可以设计出许多极点，但是有时由于运算放大器开环增益的问题会损害高频性能。常被忽视的问题是，馈入运算放大器的电流必须十分纯净。因此，这些滤波器需要一个滤波器（图 15.17）。此处有一个很多高阻线路需要滤波的例子，其中运算放大器的正负电压必须由一个 RC 滤波器或传统无源滤波器滤波，这个滤波器电容要面对负载。

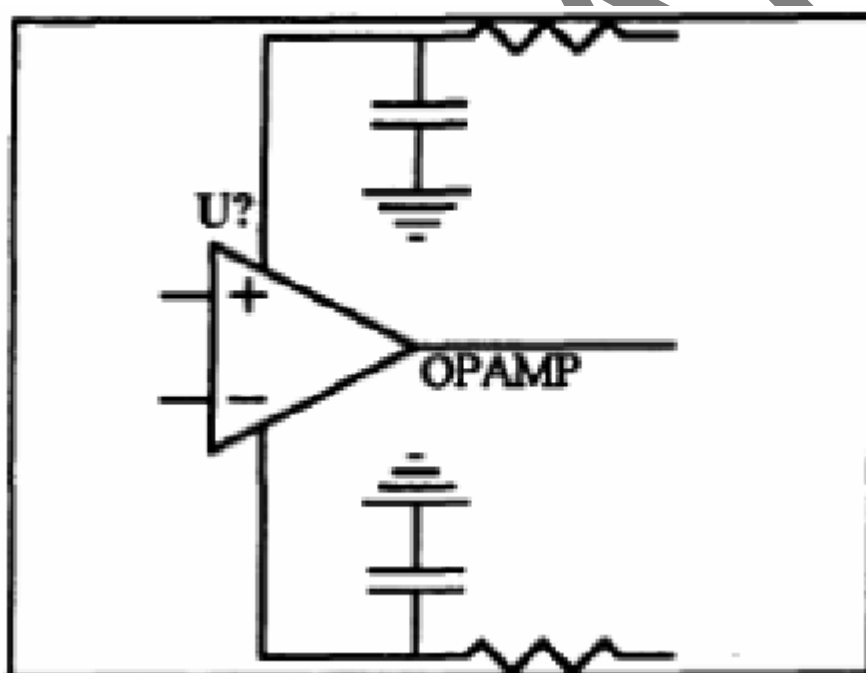


Figure 15.16 The active filter.

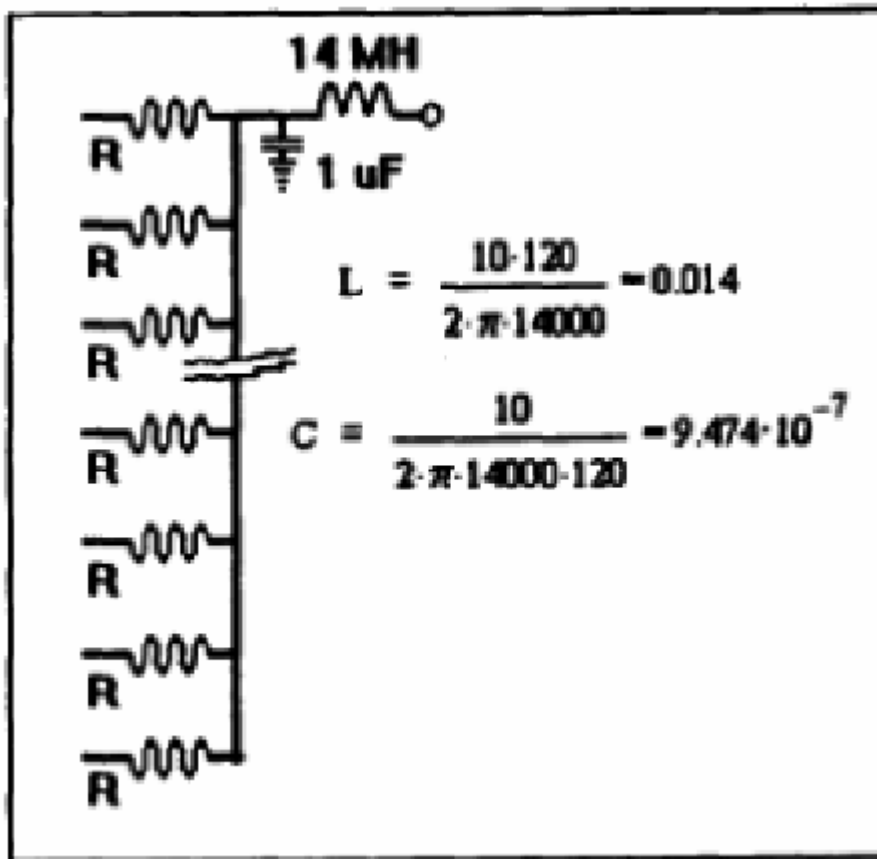


Figure 15.17 The filter required to filter the active filters.

$$R \ll \frac{B^+}{10I_{\max}} \quad (15.8)$$

If the voltage is 12 V and the maximum current is 10 mA, the maximum value of R is 120 Ω . Make R 100 Ω , and the capacitive reactance value is also 100 Ω at half the needed cutoff frequency. Note here that this gives a 1 V drop, and if this is excessive, either the resistance must be lowered or the voltage supply must be increased to allow for it. If 14 kHz is the operational ampere cutoff frequency, then at 7 kHz, C is equal to 0.22 μF ; round this to a standard value. The same is true for the other B⁺ supply. If there are a group of these, say, 10 then the total B⁺ current is 100 mA. This give an impedance of 120 Ω .

如果电压为 12V 最大电流为 10mA，则 R 的最大值为 120 Ω 。现令 R 为 100 Ω ，并且电容容抗值在需要的截止频率点的一半的频率下也为 100 Ω 。注意到此处它有 1V 压降，如果这个压降过大，那么就需要或降低阻抗或增加供电电压。如果 14kHz 是运算放大器的截止频率，那么在 7kHz 电容 C 容量取的标准值应为 0.22 μF 。对于其它的电流 B⁺ 设计方法相同。如果有一组运算放大器，如 10 个，那么总电流 B⁺ 为 100mA，此时阻抗应为 120 Ω 。

The impedance of the inductor should be 10 times the 120 Ω just calculated, and the impedance of the capacitor should be one-tenth this impedance of 120 Ω . A good quality 1 μF capacitor should remove the noise so that one

operational ampere does not add noise to the next. The inductor removes any of these signals from the main supply.

电感的阻抗应是刚才计算出的 120Ω 的 10 倍，而电容器阻抗应为此 120Ω 阻抗的 $1/10$ 。 $1\mu\text{F}$ 高质量电容应能消除这些噪声，以使运算放大器不会将噪声传递给下一个。而这个电感会消除主供电电路上的任何噪声。

§ 15.5 F_0 The Easy Way

§ 15.5 使用 F_0 的简便设计方法

The filter can almost be designed without a computer program: truly, on the beach of a desert island with wet sand and a sharp stick! In other words, filters can almost be designed without a calculator if the design is simple. This means that the design should be without RCHU or Cauer circuits. Let us look again at the single-phase section. The goal was 46 dB, with headroom, at 20 kHz. If the engineer selected the L, as before, this would give 12 dB per octave, or 40 dB per decade of attenuation. The beached engineer would use a sharp stick to write in the wet sand:

通过这个简便方法，可以几乎不使用计算机软件来设计滤波器：形象地说就是在荒岛的海滩上只用尖棒和湿沙子就能完成设计。换句话说，如果设计很简单，那么设计滤波器可以不通过计算就行。当然这意味着滤波器设计中没有 RCHU 或考尔电路。让我们再回顾一下单相滤波器那节，在 20kHz 考虑余量需要 46dB 的插损。如果选择 L 型滤波器，那么就有 12dB/倍频或 40dB/十倍频的损耗。海滩上的工程师可以用尖棒在湿沙上写下：

Frequency (kHz)	dB
20	46
10	34
5	22
2.5	10
1.25	-2

The designer divides the frequency by 2 and subtracts 12 dB for each row, opting for the single L. It is obvious at the 5 kHz, 22 dB level that a single L does not work for this 400 Hz power system. This is because the next row is half this value of 5 kHz. This figure is below the minimum of 4 kHz that should be followed for better design that keeps the filter transparent to both the line and load. Look how close lonely filter engineer was to our reading of 1260 Hz for 46 dB of loss!

如选择单 L 型滤波器，则需要设计者将上行频率除以 2 并将上行插损值减去 12dB，这样就形成了上面的表格。显然在 5kHz，22dB 的损耗水平不适合 400Hz 电源系统。这是因为 5kHz 的半值频率 2.5kHz 已经低于最小频率 4kHz 了，此频率下所有滤波器对于负载和源应该是透明的而不是 10dB。对于 46dB 插损的例子，可以看出这个孤独的海滩工程师计算出的 1.25kHz 与我们前面 1260Hz 的计算结果是多么的接近啊！

The engineer has many miles of wet sand and starts over a few feet away in clean sand with a double L at 24 dB per octave:

这个工程师还有较低长度的湿沙，现在他又在离上表几英尺远处的干净沙滩上写下了

24dB/倍频损耗的双 L 型滤波器损耗表：

Frequency (kHz)	dB
20	46
10	22
5	-2

The engineer concludes that the double L will work and that the cutoff frequency is 5000 Hz. The double-L value of F_0 was 4600 Hz, which is close. The 10Ω design impedance must also be known, so the value of the inductors and capacitors can be calculated. For the inductor, the engineer scratches the following:

此时这个工程师判断双 L 型滤波器将可以适合 400Hz 系统，并且截止频率为 5000Hz。实际双 L 型滤波器的 F_0 是 4600Hz，二者是比较接近的。 10Ω 设计阻抗也是必须给出的，因此电感和电容值就可以计算了。对于电感，这个工程师划出下式：

$$\frac{10}{2p\ 5000} = 318mH \quad (15.9)$$

and obtains 318 uH. For a balanced filter, this is divided by 2, giving 160 uH—not all that far away from the 175. Actually, the value of 3 for π would be close enough for beach work. This would have given the value of 333 uH. The capacitor followed on more fresh sand a few feet over:

结果为 318uH 的电感值。对于平衡滤波器，此值需要一分为二得到 160uH——这个值与前面计算的 175 也很接近。实际上， π 型滤波器的 3 个元件的数值非常接近沙滩上的计算结果。这个结果会是 333uH。接下来在几英尺外的新沙上写下电容容量：

$$\frac{10}{2p\ 500,010} = 3.18mH \quad (15.10)$$

The designer knows that the capacitor value can be solved by dividing the inductance value by the square of the impedance. This is 10Ω , and squared is 100 (much easier in the wet sand): again, close to the 3.5 used earlier. The designer would round this to 3.2 uF, anyway. The Zorro remains to be calculated, and the designer knows that the feedthrough limit is 0.02 uF, or paralleled, giving 0.04 uF to ground.

当然设计者知道，可以通过将电感值除以阻抗的平方根来得到电容值。此处阻抗值为 10Ω ，其平方为 100（在湿沙上很容易计算）：同样电容值的结果接近 3.5，设计者近似取其值为 3.2uF。目前 Zorro 的值还没有计算。另外，设计者同样知道穿心电容的限值为 0.02uF，或并联对地值为 0.04uF。

Frequency (kHz)	dB
50,000	46
25,000	34
12,500	22
6,250	10
3,125	-2

Note how close this is to the 3550 earlier. The Zorro inductor value follows:

注意 3125 与早期计算的 3550 是十分接近的。则 Zorro 电感值如下：

$$\frac{10}{2\pi 3125} = 509.3mH \quad (15.11)$$

and the capacitor follows but should be held to two times the maximum to ground, or 2×0.02 , or 0.04. Again, the value of π , for beach work, could be rounded to 3, but the value is 5.09 uF. Dividing the 5.093 by 0.04 tells the engineer that the capacitor is 127.32 times too large. So the beached designer multiplies the inductor by 127.32, here, and obtains 64.8 mH. This value is somewhat close to the 50.4 mH from the earlier design. This value of inductance is too large, also a conclusion in the previous design. This engineer, similarly, adds another L filter, making the common mode a double L. The double L has 24 dB of loss per octave:

同样按此方法计算电容，但是应确保最大对地电容只是电容限值的两倍，即 2×0.02 或 0.04uF。同样对于沙滩设计师 π 型的值可以近似到 3，但是实际值为 5.09uF。将 5.093 除以 0.04 得到 127.32 倍，可以看出电容太大了。此时沙滩工程师将电感乘以 127.32，得到 64.8mH。这个值有些接近早先的设计值 50.4mH。与前面的结论一样，这个电感值也太大了，所以设计者需要再增加另一级 L 滤波器，使共模电路变为双 L 型。这个双 L 型滤波器有 24dB/倍频的插损。

Frequency (kHz)	dB
50,000	46
25,000	22
12,500	-2

The calculation of the inductor follows:

电感的计算如下：

$$\frac{10}{2\pi 12,500} = 127.3mH \quad (15.12)$$

and the capacitor,

对于电容有：

$$\frac{10}{2\pi 1,250,010} = 1.273mF \quad (15.13)$$

which is 63.65 times too large compared with the total of 0.02 uF (four feedthroughs, 0.01 each), so the inductor is multiplied by 63.65, giving 8.1 mH, which is close to the earlier 7.9. Note that the impedance of the common mode filter section is no longer 10Ω .

可以看出这个电容值还是太大了，其值是总限值 0.02uF（4 个穿心电容，每个 0.01uF）的 63.65 倍，所以将电感乘以 63.65 得到 8.1mH（这很接近先前计算的 7.9mH）。注意共模滤波器电路部分的阻抗不再是 10Ω 了。

$$\sqrt{\frac{8100}{0.02}} = 636.396 \quad \text{or} \quad 10 \times 63.65 \quad (15.14)$$

and the cutoff frequency is still 12,500 Hz:

但截止频率仍为 12,500Hz :

$$\frac{1}{2p \sqrt{0.0081 \times 0.02 \times 10^{-6}}} = 12,500 \text{ Hz} \quad (15.15)$$

The final design is shown in Figure 15.18.

最终的设计见图 15.18。

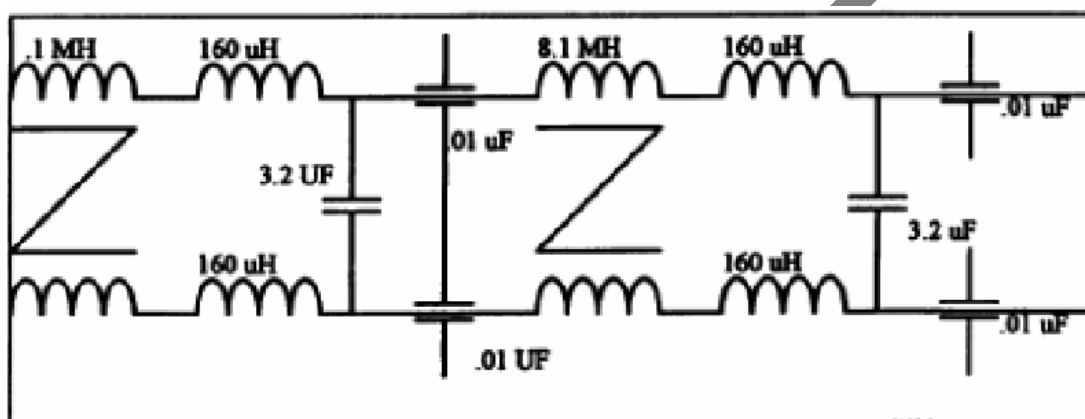


Figure 15.18 The fully designed filter using F_0 the easy way.

This technique of trading inductance for capacitance can be used in common mode filter design but not in differential, or normal, mode design because the design impedance changes. There is no need to match the impedance in common mode. Also, the two Zorros lowers the circuit Q because the inductance is so much lower than that with the single Zorro. Q was already very low in common mode. Thus, the increase does not enhance oscillation. This technique, if used in the differential mode, would raise Q in the differential mode, which is already too close to the edge of oscillation. Also, the common mode load impedance of the actual equipment, in most applications, is much higher than that of differential mode impedance. This fights against the common mode Q increase and reduces the opportunities to oscillate. The same technique works on Ts and π s, except that 18 dB is used-replacing 12 dB for the L-for each level as the frequency is divided by 2. Use 30 dB per octave for two or multiple networks, adding 12 dB for each additional network. Three networks gives 42 dB per octave. Count the elements of the entire network: the double T has five elements at 6 dB per octave each, giving 30 dB each octave. If the frequency is high enough, the decade system can be used and the decade and octave can be used together. For example, a T has 18 dB per octave and 60 dB per decade. If 90 dB is required at 160 kHz, will the filter be okay for a 400 Hz line frequency? Add 6 dB headroom for a required loss of 96 dB. The first step

was the decade followed by two steps of octaves. The filter should be okay (Table 15.1 and Figure 15.19).

当然，这种用电感值改变来补偿电容值变化方法只能用在共模滤波器设计中，而不能用在差模或常模设计中，因为这样会改变设计阻抗，而在共模中是不需要阻抗匹配的。同样，因为两个 Zorro 的电感远小于单个 Zorro，因此两个 Zorro 会降低电路的 Q 值，所以共模电路的 Q 值很低。因此 Zorro 数目的增加不会增强谐振。如果将此设计技术用在差模电路中，这将会提高已经很接近谐振边缘的差模电路的 Q 值。另外，在实际应用中，共模负载阻抗在很多情况下是高于差模负载阻抗的。这也会抵消共模 Q 值的上升，并减小谐振的几率。而对于 T 型和 π 型电路，除了在前面的列表中对每次频率减半的损耗减数要用 18dB 来替代 L 型的 12dB，其它设计方法均相同。对于 2 级或多级电路网络插损值取 30dB，每增加一级增加 12dB 的插损，因此 3 级网络插损为 42dB/倍频。数一下整个网络的元件数：双 T 型有 5 个元件，每个损耗为 6dB，总插损为 30dB/倍频。如果频率足够高，也可以使用十倍频单位或倍频与十倍频混用。例如， T 型网络为 18dB/倍频、60dB/十倍频。如果在 160kHz 需要 90dB，这个滤波器会满足 400Hz 电源线频率的需要么？先再增加 6dB 的插损余量得到 96dB 的实际插损需求。第一步取十倍频，接下来两次取倍频，通过表 15.1 和图 15.19 可以发现此滤波器满足要求。

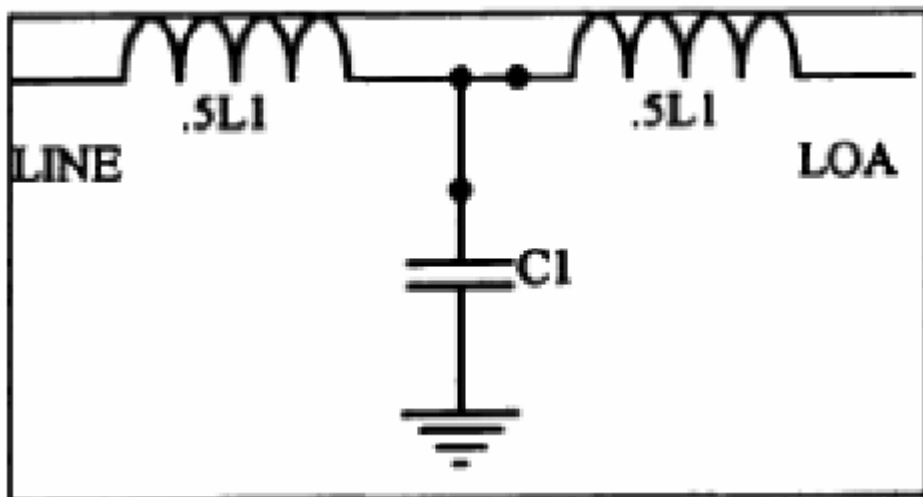


Figure 15.19 The T used to show the element count.

Table 15.1 Using the dB Loss per Decade and dB Octave Loss

Frequency	Loss
160	0
16	60
8	78
4	96

Table 15.2 dB Loss at Two Different Frequencies

Again, the filter must be checked at each frequency listed in the specification to see that the filter meets the assigned loss at that frequency. One specification was as follows: 30 dB at 100 kHz and 80 dB at 800 kHz. Adding 6 dB for headroom, 36 dB loss is required at 100 kHz and 86 dB at 800 kHz. Using the single L, the loss chart is shown in Table 15.2. Most think that the filter designed for the lowest problem frequency would be good enough to handle all the rest of the list: good odds but not always true as in the preceding example. The single L's cutoff frequency must be 5 kHz, not 12.5 kHz.

同样需要对每个频点进行检查以确保滤波器满足规格书指定的损耗。如某个规格书如下：30dB@100kHz、80dB@800kHz。增加 6dB 余量则需要 36dB@100kHz、86dB@800kHz。对于单 L 型，插损表如表 15.2。大多数人认为在最低频率满足要求的滤波器，其它频率下也没有问题。实际上这是很有可能的，但是在前述的例子中并不总是总如此。另外，单 L 型的截止频率必须是 5kHz，而不是 12.5kHz。

The easy method for the computer or calculator is as follows:

Loss required=dB

Loss per octave for filter=L

Number of octaves = X = dB/L

Frequency at needed loss = F

Cutoff frequency = $F_0 = F/2^X = F_0 = F/2^x$

一个简便的计算方法如下：

插损要求=dB

滤波器每倍频插损=L

倍频数=X=dB/L

所需插损的频率=F

截止频率= $F_0 = F/2^X = F_0 = F/2^x$

36 dB at 100 kHz		86 dB at 800 kHz	
Loss	Frequency	Loss	Frequency
36	100	86	800
24	50	46	80
12	25	34	40
0	12.5	22	20
		10	10
		-2	5

§ 15.6 Remote High-Voltage Supply Fed from a Local DC

Power Supply

§ 15.6 本地 DC 电源的远端高压供电

A very capable power supply company had a contract to design a power supply with several output voltage. One was 60 V at 0.5 A. After the design, they built and tested three and sent two to the customer for approval. After several weeks, the approval was received and the well-designed EMI filter at the power input also passed the 461 specification. A panic call came from the customer 2 days later. The request was for them also to design a remote power supply utilizing the 60 V at 0.5 A for a builtin remote monitor. This monitor power supply required 16 inches of cable. A key player had died, so this other group could not finish the design on time. The output was 20 kV at 0.8 mA. The power supply company designed a double-ended forward converter, each half conducting with a duty cycle 0.8 of its conduction time, and a switching frequency of 50 kHz. This makes the current pulses 100 kHz at an on time current of 0.625 mA. The questions are as follows:

曾有一个非常有技术实力的电源公司接到一个设计合同，需要设计一款输出多路电压的电源。其中一路是 60V@0.5A。在设计完成后，他们做了 3 个样品并寄给了客户 2 了做验证。几周后，验证结果出来了，在电源输入端口的滤波器设计得十分出色，顺利通过了 461 规范。但 2 天后客户打来紧急电话，需要为内建的远端监视器也设计一个 60V@0.5A 的远端供电电源。这个监视器电源需要 16 英寸长电缆。但是此电源关键的设计人员死了，所以其它的人无法按时完成该设计。条件是输出为 20kV@0.8mA，电源公司设计了一个双端逆变器，每个采用占空因数为 0.8 的信号，且开关频率为 50kHz。这在工作电流造成了 100kHz 的电流脉冲，问题点如下：

1. With a proper filter at the front end of the main supply, is another filter needed?
 2. Where would the filter, if needed, be located: at the output of the original supply, somewhere in the cable, or at the input of the new supply?
 3. Besides the obvious snubbers, for example, what else could be done to reduce the size and cost or to eliminate the filter?
 4. Do we care what the 60 V power supply output impedance is at 100 kHz?
- 1、在主电源前端有一个合适的滤波器的情况下是否需要另一个滤波器？
2、如果需要，那么应选在什么位置：在原电源的输出端的电缆某处或新电源的输入端？
3、例如在缓冲器旁还需要做什么才能减少滤波器的尺寸和成本，或根本就不使用滤波器？
4、我们需要关注 60V 电源在 100kHz 的输出阻抗么？

The answer to the first question is, yes, and the reason will be apparent as the other questions are answered. The second answer is, if needed, at the input of the remote supply because the current on the cable between the two supplies must be steady direct current with as little ripple as possible to eliminate radiation to other wires within the harness and also to the surrounding areas. For the third question, if the input section of the remote supply was isolated, requiring a return lead to the first supply, a twisted pair would help eliminate the radiated emissions. Although the filter is designed properly, there will be some ripple on the cable after filtering. A shielded pair would also be good, but ground

the shield only at one end. The best end would be the 60 V end, to reduce ground currents. Also, Capcon could be used to cover the wires between the two supplies and dissipate the energy.

第一个问题的答案是：是！其原因将在回答后面的问题中提到。第二个问题的答案是，如果需要滤波器那么就应将此滤波器放置在远端电源的输入口处。这是因为位于两个电源之间的电缆上的电流必须是恒定的直流，而且为了消除对同线束其它线和环绕区域的辐射需尽可能减小纹波。对第三个问题，如果远端电源的输入部分被隔离，并需要第一次电源提供一个回线，那么双绞线会较好消除辐射。尽管滤波器设计得很恰当，但在滤波后电缆上还是会有些纹波。另外，使用屏蔽双绞线也很好，但需要只对一端接地。接地最好在 60V 电源端，这样可以减小地电流。还有，可以使用 Capcon 电容来保护电源间的线缆，并能用它来消耗噪声能量。

Before the last question is answered, the following should be understood. What if the original designer knew that the remote switcher frequency was 10 kHz and designed the 60 V output impedance to be milliohms around this frequency? What would the results be? The path of least resistance for the 100 kHz current pulses is through the cable, creating high-level radiation to the surrounding media. Discounting radiation, the rest of this circuit should work fine. A filter at the input to the remote should reduce this radiation.

在回答最后一个问题前，需要了解以下知识。如果原来的电源的设计者知道远端电源的开关频率是 10kHz，并且将 60V 电源在此频率下的输出阻抗设计成毫欧级，那么结果会如何？此时 100kHz 电流脉冲的最小阻抗传输路径会是电缆，这样会对周围产生高等级的辐射。当然如果减小辐射，其余的电路就会正常工作。此时在远端电源的输入端加一个滤波器就会减小辐射。

Now the opposite condition: the original engineering group was unaware of the purpose of the 60 V, and the output impedance is 24Ω in the 100 kHz region. What are the results now? The radiation would be reduced, but the switcher may not function properly at the reduced voltage. The peak on current is 0.625 A, reducing the supply voltage to 45 V. A filter at the input to the remote should reduce this switcher droop or starvation.

现在考虑相反的条件：原电源的设计组并不知道 60V 电源供电的对象，设计的 60V 电源的输出阻抗在 100kHz 区域为 24Ω 。那么结果又如何呢？结果是辐射将会减少，但是因为电压降低使得开关电源不能正常工作。如电流的峰值为 0.625A，这样就会把供电电压减小到 45V，因此在远端电源的输入端口加一个滤波器就会降低开关低垂或“饥饿”现象。

Note that the solution to both problems is the same: a filter. A good filter reduces the peak-to-peak ripple level, reducing the radiation. This filter also reduces the output impedance to the switchers following the filter located in the remote power supply. The answer to the fourth question is , no. The system needs a filter whatever the output impedance and a filter will fix either problem. 注意，两种情况的解决方法是一样的：加一个滤波器。好的滤波器会降低峰—峰值纹波电平，并减小辐射。这个滤波器会降低它后面的开关电源的输出阻抗。第四个问题的答案是：否。无论输出阻抗如何，系统都需要一个滤波器并且此滤波器会同时解决这两个问题。

To design the filter, all the processes covered in this book could be reviewed - the dBuA/MHz, the conducted emissions, and the radiative emissions - but this takes time and involves testing costs. The filter can be designed without all this. It may require some final adjusting, but so would the system after all the time and expense.

为了设计这个滤波器，我们会回顾本书所有涉及滤波器设计的过程：dBuA/MHz、传导发射、辐射发射，而且这些设计过程需要测试成本和时间。当然设计滤波器也可以不做这些测试，而只需要做一些最终调整，但是这样整个系统会消耗测试时间和成本。

The easiest method is to divide the 60 V by the 0.625 A *on current* and obtain the on impedance of 96Ω . Divide this by 10 to obtain the filter capacitor impedance at 100 kHz of 9.6Ω . The value of the capacitor is

按最初的设计方法是，将 60V 除以 0.625A 得到阻抗为 96Ω 。将这个阻抗除以 10 得到滤波器电容在 100kHz 阻抗为 9.6Ω 。那么电容的值为

$$\frac{1}{2p \times 100,000 \times 9.6} = 0.166mF = 0.2mF \quad (15.16)$$

or round this to 0.2 uF, and choose a type having a self-resonant frequency (SRF) at least 10 times the switcher frequency. This is 100 kHz, in this case, giving 1 MHz SRF. The inductor should have 10 times the 96Ω , for this example, or 960 at 100 kHz:

或将电容值近似为 0.2uF，并且选自谐振频率至少是 10 倍于开关频率的电容。在本例中，开关频率为 100kHz，所以电容的 SRF 应为 1MHz。而电感应 10 倍于 96Ω ，也就是在 100kHz 频率下为 960Ω 。

$$\frac{960}{2p \times 100,000} = 0.002H = 2mH \quad (15.17)$$

This is split, with half on the hot side and half on the return side, 1mH each (Figure 15.20). This is a large value for the inductance but easy to design for the direct current of 0.5 A, although the SRF may fight. Raise it as high as possible.

如果采用平衡电路设计则一半电感在火线侧，另一半在零线侧，每侧 1mH（图 15.20）。这个电感的值很大，尽管 SRF 会不利于此电感设计，但对于直流 0.5A 此电感是很容易设计的。因此可以将此电感值尽可能地提高。

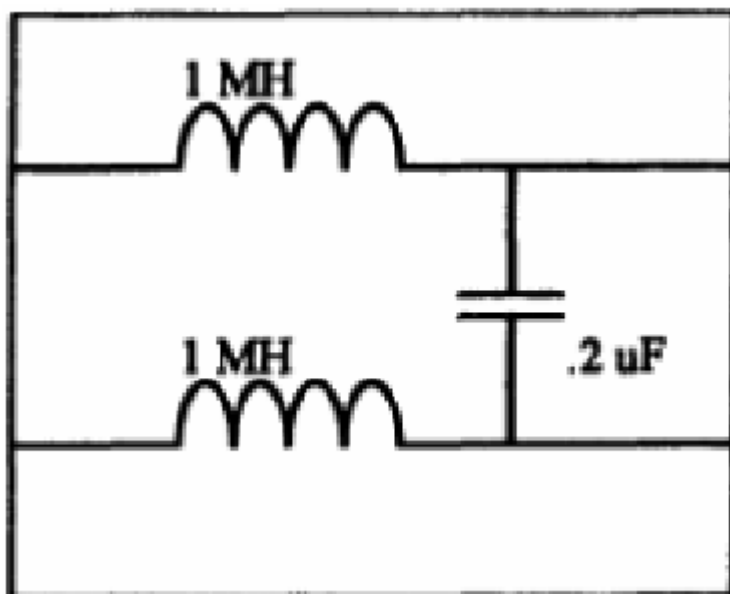


Figure 15.20 The remote filter in the monitor power supply.

The filter impedance is

此滤波器阻抗为

$$\sqrt{\frac{0.002}{0.2 \times 10^{-6}}} = 100 \quad (15.18)$$

which is close to the 96, and the cutoff frequency is

这个阻抗值接近 96, 并且滤波器的截止频率为

$$\frac{1}{2\pi \sqrt{0.002 \times 0.2 \times 10^{-6}}} = 7958 \text{ Hz} \quad (15.19)$$

The approximate loss is as shown in Table 15.3.

近似的损耗如表 15.3 所示。

Table 15.3 Approximate Loss of the Remote Filter

Frequency	dB
8,000	0
16,000	12
32,000	24
64,000	36
100,000	42

This should knock the socks off the radiative emissions and give a

low-impedance source to the switcher. The pulse power is

这个频率正好落在辐射发射频率外，并且给开关电源提供了一个低阻抗源。其中脉冲功率为

$$20\log\frac{2EA\times10^6}{T} \quad (15.20)$$

which equals

它等于

$$20\log\frac{2\times0.625\times8\times10^6}{10}=120dB \quad (15.21)$$

The 20 dB per decade starts at

20dB/十倍频的插损的起始频率为

$$\frac{1}{pa}=\frac{1}{p8\times10^{-6}}=39,789Hz \quad (15.22)$$

which is 39.789 Hz, and the level at 100 kHz is

在 100kHz 其电平为

$$20\log\frac{1}{pFa}=20\log\frac{1}{p10^5\times8\times10^{-6}}=-8dB \quad (15.23)$$

where a is in seconds and F is in Hz.

此处 a 的单位是秒，F 的单位是 Hz。

With -42 approximate loss in the filter and -8 from the wave, the full loss would be -50. Subtracting this from 120 would leave 70 dBuA. This should be adequate because this is not on the power line. What does radiate is reduced by distance. However, this may still be out of specification depending on the requirements of the specification. If this is out of specification, add the shielded balanced cable first, with the ground at the initial supply end. If the system still fails, add another, identical filter. This should give another -42 dB, so now the level is around 30 dBuA, and this must be adequate. Do not try to solve this problem by gonging to a double L with smaller values. This could work, but the dc voltage drop feeding the switcher could be excessive.

滤波器损耗为-42dB 且波幅为-8dB，则总损耗为-50dB。从 120 减去这个损耗剩下 70dBuA。这就足够了，这是因为这个电流不在电源线上，而且辐射会因为距离增加而衰减。然而，这个结果或许还不能满足需求规格的要求。如果满足规范要求，则第一步先加平衡屏蔽电缆，其屏蔽层在原电源处接地。如果仍不满足，再加一个同样的滤波器。这个滤波器会再给出一个-42dB 的损耗，此时噪声电流为 30dBuA，这一定足够了。另外，不要试图通过小参数值的双 L 型滤波器解决此问题，这样虽然有用，但是馈入开关电源的 DC 电源的电压降就太大了。

16

Applications Using Round or Square Conducting Rods

圆或方导电轴杆的应用

Two similar conditions are treated here. The first is the very high current filters based on toroids and round conducting rods through them. The capacitors are the feedthrough type, also threaded onto the same conductive rod. The second method uses square conductive rods, but the capacitors are not centered on the rods as in the first method. They are 90° to the rod, and the feedthrough bolts are threaded through holes in the conductive bar. In both cases, the conductive rod, or bar, is made of material other than copper because of the strength required to support the torque caused by the nuts if these bars are extended through the case. This is especially true in the first example discussed here. Make sure to use a large enough bus, or bar, so the heat rise is low. The capacitors either surround this bus or are tightened against it, in the second system, and thus the bus temperature must be low. This chapter discusses their major disadvantage. The best solution is not to require them! Several issues are discussed here, with some ideas on how to design around them if the need arises.

此处讨论的是两个相似的使用情况。第一种是使用圆导电轴杆穿过磁环的大电流滤波器。电容是穿心型也穿在此导电轴杆上。第二种方法是使用方导电轴杆。但是电容就不能像第一种方法那样穿在导电轴杆上了，这些电容与轴杆成 90° 夹角，并且其穿心螺柱穿过导电轴杆上的孔。对这两种使用情况，如果导电轴杆延伸入并穿过滤器壳体，那么就需要轴杆具有能承受螺母的扭矩的强度，因此导电轴杆往往不能使用铜来制作，对第一种使用方法尤为如此。同时还需要确保使用足够大的导电轴杆以降低温升。电容的安装要环绕导电轴杆或对于第二种使用方法把电容紧密连接在轴杆上面，这样就要求导电轴杆温度必须很低。本章讨论的是它们的主要缺点，最好的解决方案并不需要导电轴杆。此处也会讨论几个这样的解决方案，并在如何设计环绕导电轴杆上给出一些思路。

§ 16.1 Very High Current Filters

§ 16.1 极高电流的滤波器

First we review the number of filters in cascade or tandem. If Q is low enough, the number of resonant rises is one less than the tandem number in most applications. The maximum is normally four multiple filters in tandem, which should yield three resonant rises. This holds only if Q is low enough; otherwise, there are the four resonant rises. In high-current filters, the rule of a maximum number in cascade, or tandem, is broken for several reasons. The new maximum number is seven filters in tandem. For example, there could be seven

L filters, one after another. This gives six potential resonant rises if Q is low enough. One reason for the exception of a maximum of four in cascade is the high capacitor values required for proper design. They become very unrealistic, and the self-resonant frequency (SRF) drops to low values for the two, three, or four cascaded filters. As the number in tandem increases, the capacitor value decrease. Inductor values have the opposite problem. They shrink in value, into the low uH range. To fix this low-value problem of the inductors and to reduce the size of the capacitors, a second idea must be discussed: paralleling the filters. If the number in parallel is N, the impedance of each unit in parallel is multiplied by N. The value of the inductors is N times large, and the value of each capacitor is divided by N. The impedance of each filter unit in parallel is

首先我们来回顾一下前后层叠连接的滤波器的个数。如果 Q 值足够低，那么在绝大多数应用中谐振增益的个数会是滤波器层叠个数减 1。通常最大级数的滤波器是 4 级滤波器，此滤波器会产生 3 个谐振增益点。注意，以上成立的条件是 Q 值足够低，否则就会因为几个其它的因素而打破滤波器最大前后层叠数目的规则。如一个前后层叠数为 7 的滤波器，可能它有 7 个 L 型滤波器电路前后相连。如果 Q 值足够低，那么此滤波器就有 6 个潜在的谐振增益点。导致 4 级滤波器出现例外情况的一个原因是，设计所需要的大电容值。对于 2、3 或 4 级滤波器电容值大得不切实际，并且自谐振频率值很低。因此当层叠数增加时，需要电容值降低。电感的情况是，它们的值缩小到 uH 范围。为了解决电感值降低问题并减小电容尺寸，需要讨论第二种应用思路：并联滤波器。如果并联数为 N，那么每个并联的滤波器单元的阻抗应是原滤波器阻抗的 N 倍。这相应地要求滤波器单元的电感是原来的 N 倍，而每个电容是原来的 1/N。这样每个并联的滤波器单元的阻抗为

$$\sqrt{\frac{NL}{C/N}} = \sqrt{\frac{N^2 L}{C}} = N \sqrt{\frac{L}{C}} \quad (16.1)$$

and the parallel filter impedance is the same as the initial impedance because N are in parallel.

因为 N 个滤波器并联的原因，这个总并联滤波器阻抗会与原来的阻抗相同。

Another solution to the high-current filter is not to filter it! Filter the lower current areas. The U.S. Army Corps of Engineers consistently ignores this idea. They wanted an entire power line, with currents of 600, 800, and 1000 A per phase, to be filtered rather than to filter the distribution legs, which would have been easier. It is likely that the entire volume and weight of the branch filters would have been less than that of one big filter. These branch filters would probably have cost less, also. The quality of the filter's ability to operate at higher frequencies, because of the improved SRF values, would also have greatly increased.

对于大电流滤波器的另一个解决方案是根本不滤波，只分别对低电流区域滤波。但美国军用公司的工程师一直忽视这种方法。他们总是想对每相承载 600、800 或 1000A 电流的整个主电源线进行滤波，而不是只对每个分支的配电引线进行滤波。很可能每个分支滤波器的重量和体积之和还小于一个大的主路滤波器的重量和体积。这些分支滤波器很可能成本更低，同样分支滤波器的高频性能也会明显提高。这是因为分支滤波器改良了 SRF 值。

Another costly solution is to use transformers to step up the voltage and step down the current. This raises the design impedance, making the components much more realistic. The higher design impedance increases the value of the inductors, making them more realistic. This also holds true for the capacitors and makes for smaller, more realistic capacitor values. Both components would have better SRF values. Note the second word, cost. These filters cost like gold, anyway, so two transformers on opposite ends may not affect the price too much. Another method may be to filter the power before the step-down transformer to save the cost of one transformer (you require this transformer, anyway). The input transformer is either a Y to Δ or Δ to Δ . Another advantage to adding the two transformers is that the neutral current caused by unbalanced currents on the neutral is eliminated. This is true of all the harmonics that are multiples of 3, especially the third harmonic current. These add in-phase on the neutral, along with the neutral unbalanced current, and are eliminated. Filtering this as a three-phase three-wire Δ would also end the requirement to filter the neutral, which must be as large as the filters in the other legs. (See Section 15.2 for more information.) Carry the ground wire through to these filters because they must be well grounded to function properly. The cost saved by eliminating the fourth neutral filter helps to offset the transformer cost if this technique is used. The current in each leg will still be high and may require several filters in parallel besides the transformer(s) technique.

另一个昂贵的解决方案是使用变压器来提高电压并降低电流。这将会提高设计阻抗使元件值更切实际。高阻抗设计提高了电感值使得此值更切实际。同样对于电容也会有效果，会使电容值降低为更实际的电容值。而此时两种元件都会有较好的 SRF 值。但采用这种方案要注意成本问题。由于那些高电流滤波器的成本就像用黄金制作的一样高，所以在两端增加变压器无论如何都不会明显影响价格。另一个办法是可以在降压变压器前滤波来节省变压器成本（无论如果你还是需要这个变压器的）。输入变压器类型可以是 Y- Δ 型或 Δ - Δ 型。增加此二变压器的另一个优点是，可以消除不平衡电流导致的零线电流。同样此变压器可以消除 3 的倍数次谐波，尤其是 3 次谐波电流。另外还会消除同步施加在零线的谐波和非平衡电流。将之设计为类似于三相三线 Δ 型滤波同样也会不需要零线滤波，而这个省去的零线滤波器会与其它相线的滤波器一样大（15.2 节会有更多的叙述）。因为滤波器需要良好接地，所以要将地线穿过这些滤波器。如果使用了加变压器的方法，省去零线滤波器会有助于降低变压器成本。如果不使用加变压器的方法，那么每相电流仍会很高，而且会需要几个滤波器并联结构的滤波器。

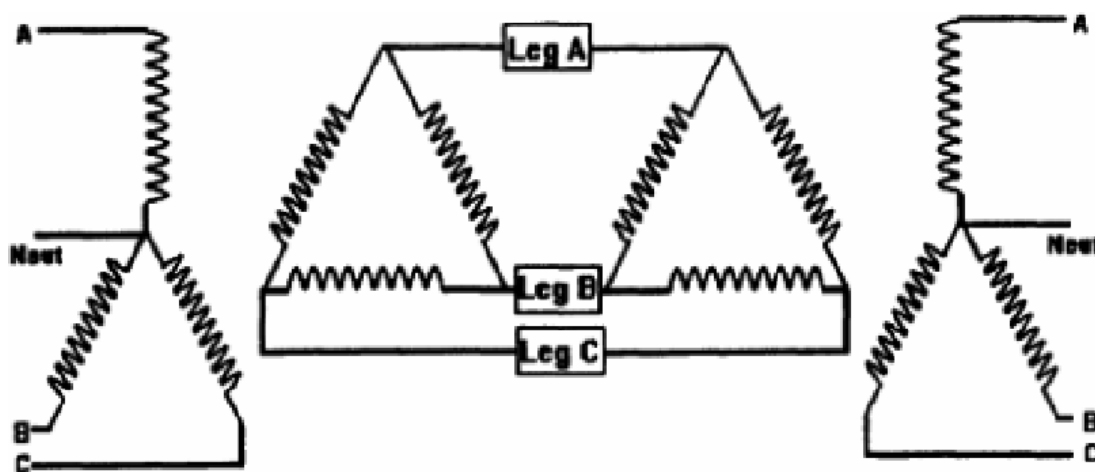


Figure 16.1 The step-up and step-down transformer for lower current filtering.

The following discussion is based on approximations that are useful to design the filter quickly. The values can be moved later once they are at least ballpark property if not on the playing field.

以下基于近似的论述会有助于快速设计滤波器。一旦它们的特性不符合应用领域，这些值是可以修改的。

The cutoff frequency F_0 , the value of the inductance in microhenries, and the value of capacitance in microfarads are listed in Table 16.1 for 440 V, 400 A at 400 Hz requiring 100 dB at 14 kHz. These values were calculated using the methods discussed earlier with matrix algebra. The design impedance is 440 divided by 400, or 1.1, and multiple Ls were chosen.

对于 440V/400A@400Hz 在 14kHz 频率下需要 100dB 插损的情况，所需滤波器的截止频率值、电感值 (uH) 和电容值 (uF) 都列在表 16.1 中了。这些值是用前面论述的矩阵代数方法计算出来的。其中设计阻抗为 440 除以 400 等于 1.1。另外，此处选择的是多 L 型滤波器。

Table 16.1 High-Current Unparalleled Filter Values

Number of elements	Cutoff frequency F_0	Inductance	Capacitance
5	3750	46	38.5
6	4500	39	32.5

The cutoff frequency of the five L filters in tandem is somewhat low for 400 Hz. This makes the six-element filter the better choice. Look at the value of the capacitors required for either the five- or six-element filters, however. This would require five or six capacitors this size (and inductors) to make up the filter.

These values for the capacitors are may too high. Even if two capacitors are paralleled, 20 uF for the five element and 16 uF for the six element, the SRF would be too low. The SRF of each capacitor would be in the low-frequency area, around 60 kHz or lower, depending on the type of capacitor chosen. Paralleling the entire filter would aid in solving this problem, as suggested by Table 16.2. The design impedance is now 4.4Ω , with four in parallel, and the current is now 100 A. This would form a two by two, giving four filters in parallel. With this low a current (100 A per filter in parallel), a conventional design could be used.

5 级 L 滤波器对 400Hz 应用来讲其截止频率显得有些低。然而就 5 或 6 级滤波器所需要的电容值来看, 选 6 级的滤波器会较好。因此就需要 5 或 6 个这样大小的电容 (和电感) 来制作这个滤波器。注意这些电容值太大了, 甚至对于采用两个电容并联的方法, 5 级滤波器 20uF 和 6 级滤波器 16uF 的电容的 SRF 还是太低了。每个电容的 SRF 都处在低频区域, 随着电容类型选取的不同, 其值为 60kHz 左右或更低。按表 16.2 的建议, 并联滤波器设计方法可以解决这个问题。现在 4 个滤波器并联后设计阻抗为 4.4Ω , 电流为 100A。对于这种低电流滤波器 (每个并联滤波器 100A 电流), 可以使用常规的设计方法。

Table 16.2 High-Current Four-in-Parallel Filter Values

Number of elements	Cutoff frequency F_c	Inductance	Capacitance
4	3000	233	12.0
5	3950	177	9.2
6	4600	152	8.0

Four elements is much too low to consider; five elements is okay. The advantage of six elements is that the capacitance is reduced from 9.2 to 8 uF, for a somewhat higher SRF, and the same is true of the inductance. It is obvious that this solution means a large number of elements. If the filter engineer opts for the six-element filter, this equates to six by four inductors at 152 uH and six by four capacitors at 8 uF, or a total of 48 components. Big? Yes! Heavy? Yes! Costly? Yes! (And I hope you have to build more than one to help offset the design costs!)

4 级滤波器的截止频率太低, 而 5 级则符合要求。但是如果使用 6 级滤波器会有令电容值从 9.2 降低到 8uF 的优点, 这样电容的 SRF 就会高些。当然对于电感同样如此。显然此解决方案意味着需要更多的元件。如果选择了 6 级滤波器, 则需要 6×4 个 152uH 的电感和 6×4 个 8uF 的电容, 总共需要 48 个元件。太大了? 对! 太重了? 对! 太贵了? 对! (当然我希望能一次多制作几个滤波器, 这样会有助于降低成本。)

This is the disadvantage of high-current filters. The best solution is to bring this power into service and then filter the individual feeds after each breaker. The current falls, requiring fewer elements in each filter and ending the possible

need for the two transformers and the need to parallel the filters. Some designers prefer the opposite technique, to filter feed the breaker so that the filter is always alive. This means that the distribution bus feeds the filters and the filters feed the breakers. The reason is that in most designs the capacitors in the filters feed the breakers. The reason is that in most designs the capacitors in the filters are too large, and this creates difficulty in turning the power on because of the added inrush of filter current. Look at Equation (16.2), where six 32.5 μF capacitors are in parallel. The inductor furnishes low inductive reactance at the power frequency, so these give little isolation between the capacitors. This gives a total of approximately 195 μF . This capacitance plus the normal inrush may cause a breaker trip problem, but many designs have more capacitance, adding to the problem.

这就是大电流滤波器的缺点。最佳的解决方案是在每个断路器后为每个单独的电源支路滤波。这样滤波器的电流就会下降、每个滤波器会只需要很少的元件，而且不需要那两个变压器，也不需要并联滤波器了。一些设计者这会偏爱在断路器前装滤波器，这样滤波器就总处在工作状态。这就意味着供电支路馈电给滤波器，而滤波器再馈电给断路器。但是在许多滤波器中是电容馈电给断路器的，而且此电容值往往还很大，这样由于增加了滤波器涌入的电流，开/关电源就会很困难。如式 (16.2) 有 6 个 32.5 μF 电容并联，而电感在电源线频率表现为低感抗，所以电感对电容几乎产生不了隔离作用，因此电容值可以近似相加在一起为 195 μF 。此总电容产生的涌入电流会导致断路器失效，但是目前还有很多设计仍错误地在使用很大的电容，这常常引起断路器失效的问题。

If the engineer is stuck and must design this system, some ideas follow. The current-carrying elements is of bronze or brass, for example, rather than a wire or wires. The conductor rod should be round. Copper comes to mind, but it may not support the end nuts, placing too much tension on each threaded end. This stronger conducting material is often plated with copper or silver. This improves the current-handling ability of the rod. The bar or rod should have a diameter specified to handle the current flow with little heat rise. The conductor is not insulated. Both the inductor and capacitor I_d should fit easily over the conductor without being too loose. The capacitors should be the feedthrough type, with the arbor inside diameter a tad larger than the rod. The inductor is also a toroid, with the inside diameter slightly larger than the rod. These are slipped onto the rod to make the filter elements. N , the number of turn(s) of the inductor, is equal to 1. This is a copper-or silver-plated rod, with a 95% or better fill factor compared with the typical 40% for toroids. This bus runs through the inside diameter of the toroid as well as the capacitor. Later in this chapter the copper bus bar is discussed.

如果工程师还是必须要设计这个大电流滤波器系统，那么需要参照以下方法。电流承载件需要用青铜线或黄铜线而不是铁线等金属线。导电轴杆应是圆形的，首先想到的是使用铜材，但是由于铜一般不能承受终端螺母的扭矩，所以实际上会使用黄铜或青铜。这种较好的导电材料还常常电镀上银或铜来增强轴杆的导电能力。轴杆应选取在额定电流条件下满足很小温升条件的直径。轴杆应是不绝源的，并且电容和电感都可以很容易地安装在轴杆上，而不会松动。电容应该是穿心型，其芯轴直径应略大于轴杆。电感是环形的，内部直

径要略大于轴杆。这些元件穿到轴杆上就形成了滤波器的各个元件。此时，电感的匝数 N 等于 1，这个镀银或铜的轴杆使得磁环的填充因数为 95%，而不是磁环典型的填充因数 40%。这个轴杆是穿过电容和磁环内径的。在本章后部会论述铜轴的情况。

The *approximate* design equations for these high-current filters follow. The inductance is

大电流滤波器设计的近似公式如下，电感为

$$L = \frac{0.4\pi U_e A_c N^2 \times 10^{-8}}{M_{pl}} \quad (16.2)$$

where N is now only one turn, A_c is the cross section of the core (times a stacking factor S_f), and U_e is the effective permeability, M_{pl} is the magnetic path length. The core is tape-wound silicon steel that has a "Soft core" for its BH curve (Figures 16.2 and 16.3). This inductor should not be made using square-loop material. The tape thickness should be a size smaller than the size required for the line frequency. This is to prevent core losses at the harmonics of the line frequency and harmonics from any off-line regulators. Otherwise, the high harmonic current heats the core, requiring a larger core. Trade-offs of this type are discussed later. This toroid should also be gapped by the core manufacturer so that the peak current does not saturate the core. This can be determined from the BH curve, where

此处 N 仅为 1 匝，是磁环截面积 A_c （乘以占空因数 S_f ）， U_e 是有效磁导率， M_{pl} 磁路长度。磁环为缠带式硅钢片，它具有“软磁”BH 曲线（图 16.2 和 16.3）。通常这种电感不能使用方框型磁材料。缠带的厚度应小于电源线频率要求的尺寸。这是为了减小基于电源线频率的谐波或离线条件器的谐波所引起的磁芯损耗。否则高谐波电流将导致磁环过热，这样就只好更换更大的磁环。有关此类的折衷将在后面讨论。这种磁环同时应由生产商开气隙，这样峰值电流就不会使磁环饱和。磁环饱和性能是由 BH 曲线决定的，此处

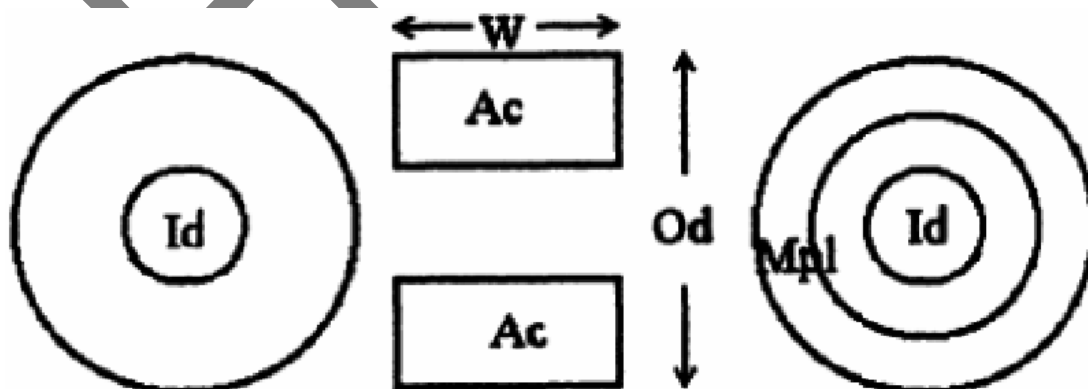


Figure 16.2 The tape wound toroid showing I_d , O_d , A_c and M_{pl} .

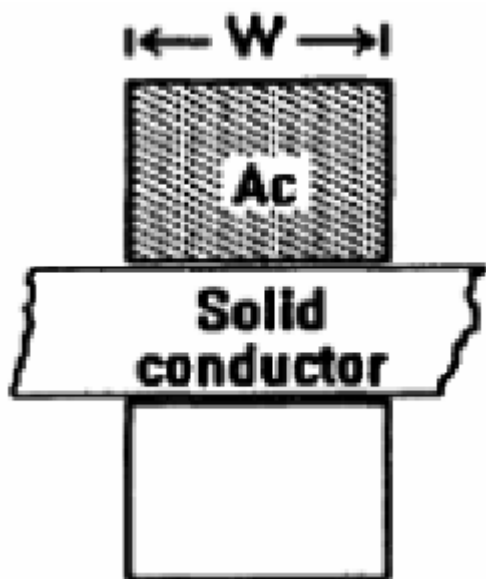


Figure 16.3 The toroid inserted in the copper bar.

$$H = \frac{0.4pNI_p}{M_{pl}} = \frac{0.4p\sqrt{2}I_{rms}}{M_{pl}} = \frac{1.7772I_{rms}}{M_{pl}} \quad (16.3)$$

because N is equal to 1. The last two equations imply that the majority of the current passing through this filter must be close to unity power factor and the off-line regulators are in the minority. If this is not true, the value of H is higher. This core should be coated with insulation (some houses use only quality tape), and the inside diameter must be maintained so that the toroid does not slip over the conducting rod with ease. Then,

式中 N 等于 1。最后两个等式表明通过滤波器的主要电流的功率因数一定要接近 1，而离线调节器的功率因数小于 1。如果事实不是这样，那么 H 的值会较高。另外，这个磁环应覆绝缘涂层（一些设计室则仅使用高质量缠带），同样内径也需要绝缘层，这样磁环就不会轻易在导电轴杆上滑动。则，

$$A_c = \frac{S_f W (O_d - I_d)}{2} \quad M_{pl} = \frac{p (O_d + I_d)}{2} \quad (16.4)$$

where the units are centimeters.

此处的单位是厘米。

$$L = \frac{0.4U_e (O_d - I_d) W S_f \times 10^{-8}}{(O_d + I_d)} = 0.4U_e W S_f \times 10^{-8} \quad (16.5)$$

where the $O_d \gg I_d$. Watch this: the poorer the conductive material, the larger the I_d must be to handle the current so that the bus does not have excessive heat rise. This heat rise can destroy the capacitors. The dimensions are still centimeters. The I_d is the diameter + of the conductor, and O_d is the maximum

allowable diameter based on the size of the insert or filter box. The amount of inductance is known because it was previously calculated. The effective permeability U_e approaches

此处 $O_d > I_d$ 。注意：导电性越差的材料为避免温升过高就需要越大的 I_d 来处理电流。温升过高是会损坏电容的。此处器件尺寸的单位仍是厘米。 I_d 是导电轴杆的直径， O_d 是滤波器外壳所允许的最大直径。电感值是已知的（很容易计算），有效磁导率 U_e 近似等于

$$U_e = \frac{U_m M_{pl}}{M_{pl} + g U_m} = \frac{p O_d}{2g} \quad (16.6)$$

where g is the gap, also in centimeters, and U_m is the core permeability. This equation is based on U_m in the tens of thousands range. The right side of the denominator of the center equation is much larger than the left-hand term. Replace M_{pl} with Equation (16.4) and substitute U_e into Equation (16.5):

此处 g 是气隙长度，单位也是厘米， U_m 是磁环的磁导率。这种近似是基于 U_m 为好几万的条件的。中间等式的分母的左一项远大于右一项。用式 (16.4) 带入 M_{pl} 并将 U_e 带入式 (16.5) 得：

$$L = \frac{0.4 p O_d W S_f \times 10^{-8}}{2g} \quad (16.7)$$

This is the individual value of each inductor used to make up the filter (six of them in the preceding case, before paralleling). Changing O_d , W , and g to inches,

这是组成滤波器的每一个电感的值（不采用并联滤波器结构，在前面的例子中是 6 个）。将 O_d 、 W 和 g 的单位换成英寸。

$$L = \frac{0.2474 O_d W S_f \times 10^{-8}}{g} \quad (16.8)$$

Solve for the width, in inches, of the inductor. For the toroid specification used here, the toroid dimensions given are O_d , I_d , and height. The W used here is the height.

现在，求解电感的宽度（单位英寸）。对于圆型环，其给出的尺寸为 O_d 、 I_d 和高度。此处用的 W 是表示高度（亦称为磁环的宽度—译者注）。

$$W = \frac{4.043 L g 10^8}{O_d S_f} \quad (16.9)$$

This way, the width of the inductor core, in inches (here, the width is the height of the core; there is only the conductor rod through the I_d), can be found to meet the required inductance. Make g vary with O_d so that g/O_d is a constant for each filter in parallel. This way W varies with L . The stacking factor S_f varies with the tape thickness only.

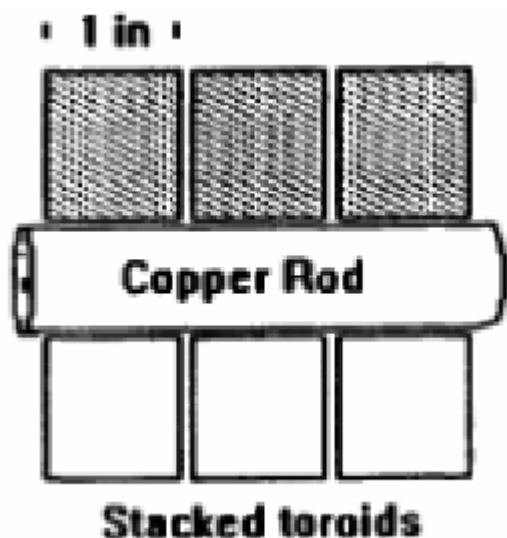


Figure 16.5 The stacking of tape-wound toroids on the copper-plated rod.

Each toroid, or C core, is insulated from the rod or bus and from each other. National-Arnold gaps the toroid, as in Figure 16.6, by slitting it, filling the gap, and coating the toroid so that the gap defies detection.

每个圆环或C型环都应对导电轴杆绝缘,而且彼此也应绝缘。National-Arnold 按如图 16.6 所示的纵切磁环方法来为磁环开气隙,然后再填充气隙并覆涂层,所以很难发现气隙。

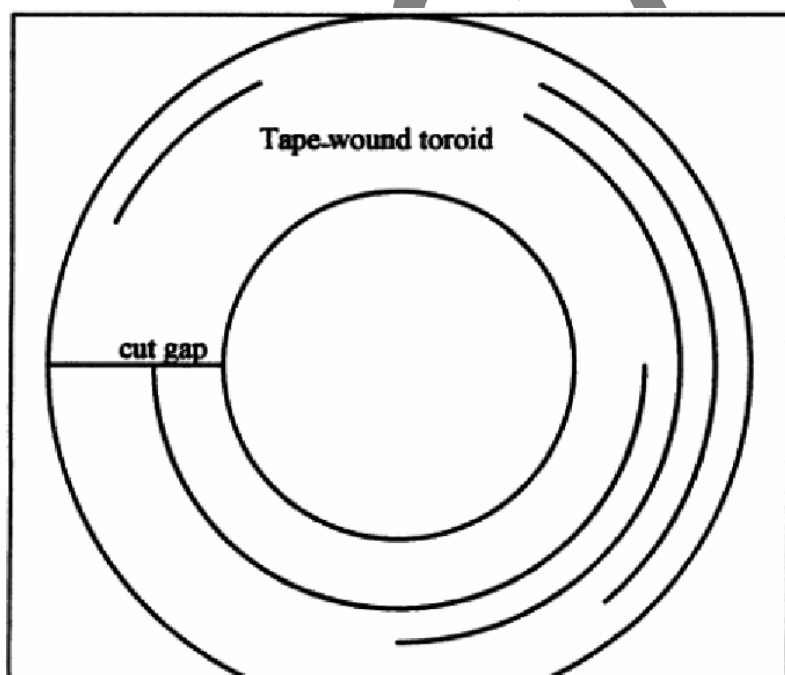


Figure 16.6 The tape-wound core gapped by National-Arnold.

The I_d and O_d of the feedthrough capacitor in Figures 16.7 and 16.8 are the same as the inductor just calculated.

图 16.7 和 16.8 中的穿心电容的 I_d 和 O_d 与刚刚计算过的电感的方法相同。

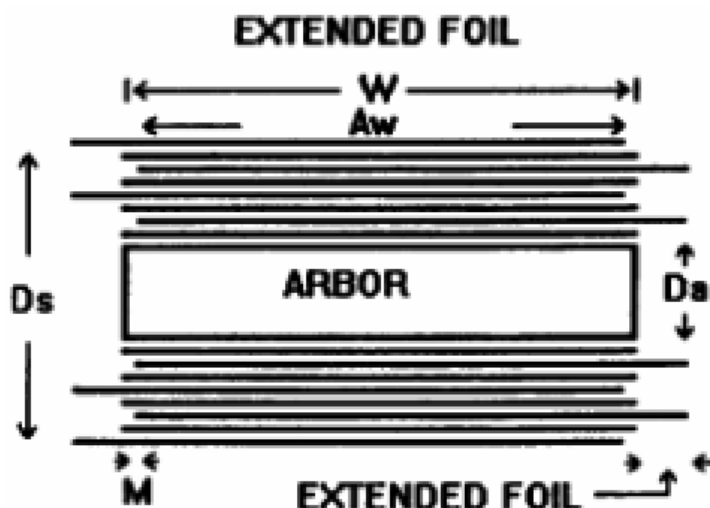


Figure 16.7 The extended foil capacitor.



Figure 16.8 Enlargement of capacitor plates and dielectrics. T is the dielectric thickness in mils while t is the thickness of two dielectrics and two foil plates thicknesses in inches.

The width must also be found. (See Section 6.2, mostly repeated here.) D_s is the outside diameter, D_a is the diameter of the arbor and t is the thickness, all in inches. D_s is the outside diameter O_d , and D_a is the inside diameter I_d . Make D_a , or I_d , slightly larger than the conductor rod and D_a , or O_d , equal to the same diameter as the high-current inductor just calculated.

同样也必须算出宽度（见 6.2 节，此处多是重复前面的内容）。 D_s 是外径， D_a 是轴内径， t 是厚度，所有这些参数单位均为英寸。 D_s 是外径 O_d ， D_a 是内径 I_d 。令 D_a 或 I_d 略大于导电轴杆，且 D_a 或 O_d 等于刚计算过的大电流电感的直径。

Solve for the number of turns N :

求解匝数 N ：

$$N = \frac{D_s - D_a}{2t} \quad (16.10)$$

Solve for the mean diameter D_m :

求解平均直径 D_m ：

$$D_m = \frac{D_s - D_a}{2} \quad (16.11)$$

Solve for the mean length of turn L_m :

求解平均匝线长度 L_m :

$$L_m = pD_m \quad (16.12)$$

Solve for the active length L_t :

求解有效长度 L_t :

$$L_t = NL_m \quad (16.13)$$

Substituting Equations (16.10), (16.11), and (16.12) into Equation (16.13),
将等式 (16.10)、(16.11) 和 (16.12) 带入 (16.13), 得

$$L_t = p \frac{D_s^2 - D_a^2}{4t} \quad (16.14)$$

To continue, we need to know the K value of the chosen material and find the dielectric thickness in mils. Values of K are also a function of shape, and the dielectric is often chosen based on the dissipation factor and size. Mylar gives the smallest dissipation factor within its normal temperature range:

接下来, 我们需要知道选定材料的 K 值和以 mil 为单位的介质厚度。其中 K 值也是形状的函数, 且介质的选择常常是基于耗散因数和尺寸的。在通常的温度范围内 Mylar 具有最小的耗散因数:

Polyester (Mylar), 900

Polycarbonate, 840

Paper (resin or PBT), 580 (wet)

聚酯 (Mylar) : 900

聚碳酸酯 : 840

纸 (树脂或 PBT) : 580 (湿)

Solve for the active width A_w :

求解有效宽度 A_w :

$$A_w = \frac{CKT}{L_t} \quad (16.15)$$

where T is the thickness of the material in mils, C is the capacitor value in uF, and K is the dielectric constant from before. Substituting Equation (16.14) into Equation (16.15).

此处 T 是以 mil 为单位的材料厚度, C 是以 uF 为单位的电容值, K 为介电常数。将式 (16.14) 带入式 (16.15) 得

$$A_w = \frac{4CKTt}{p(D_s^2 - D_a^2)} \quad (16.16)$$

If D_s , the O_d of the inductor, and D_a , the I_d of the inductor, have been chosen, the

width to be allotted for this capacitor can be found. This equation helps to find the width required to fit the capacitor. The final width will be slightly larger than $A_w + 2M$, where M is the margin for corona. The extra width allows for the extended film foldover and sputtering. This conductive tab should be soldered to the conductive bus bar, and the same style of tab should be soldered to the ground end of the capacitor (Figure 16.9). This should be soldered to a ground lug or to the enclosure wall. Some extra width should be allowed for the two tabs. The tabs must carry the capacitor current, not the full current of the filter section.

如果 D_s ——电感的 O_d 和电感的 I_d —— D_a 已选定，那么电容所能分配到的宽度就确定了。这个等式会有助于求出装电容所需的宽度。最终的宽度会稍大于 $A_w + 2M$ ，此处 M 为环状穿心电容的宽度余量。这个额外的宽度主要是用在延伸膜和真空喷镀型电容上的，图中那个导电的突起是用来焊接导电条的，而另一个同样类型的突起用来焊接电容的接地端的（图 16.9）。这个接地端应焊连接地引线或直接焊接在壳体壁上。因为这两个突起就需要一些额外的宽度。另外，这些突起必须能承载电容电流而不是整个滤波器的电流。

Figure 16.9 shows how the capacitor was slipped onto the conductor (following an inductor) and soldered to several ground points, first to the ground lugs and then the other side was soldered to the center conductor. A toroid is slipped onto the conductor afterward. The inductor is coated so that voltage is not present on the surface of the core. This continues until all the components are slipped over the conductor. Another way to mount the capacitor is to solder or sweat the capacitor to a partition that helps to isolate the compartments and forms a screen and shield. These are slipped down the conductor, the capacitor first, and the shield is soldered in place to the container. Be careful not to heat this to the point at which the capacitor solder melts, disconnecting the capacitor from the shield: spot welding may be better (see Figure 16.10).

图 16.9 表示的是电容如何穿在导电轴杆上（接下来安装电感），并焊接几个接地点：首先是接地引线，接下来是焊接在中心导电轴杆上的另一端。在电容后穿在导电轴上的是磁环，此磁环经过绝缘覆膜，所以磁环上无电压。继续将所有的元件都穿在轴上。安装电容的另一个方法是将电容熔焊在用来隔离出空间的屏蔽面上，再将屏蔽面焊接在壳体上。注意不要加热焊接电容的地方，这样会使焊接电容的焊锡融化，导致电容与屏蔽面分离，实际上采用点焊效果更佳（见图 16.10）。

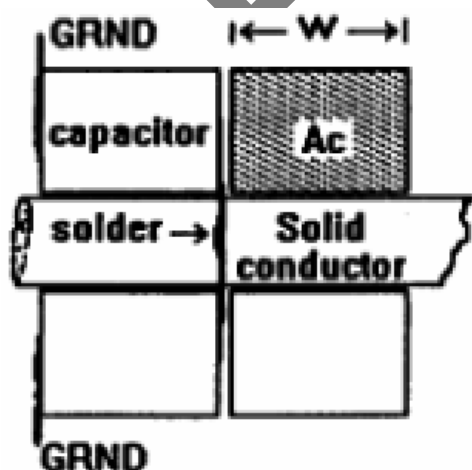


Figure 16.9 The stacked capacitor and inductor on the copper conductor rod.

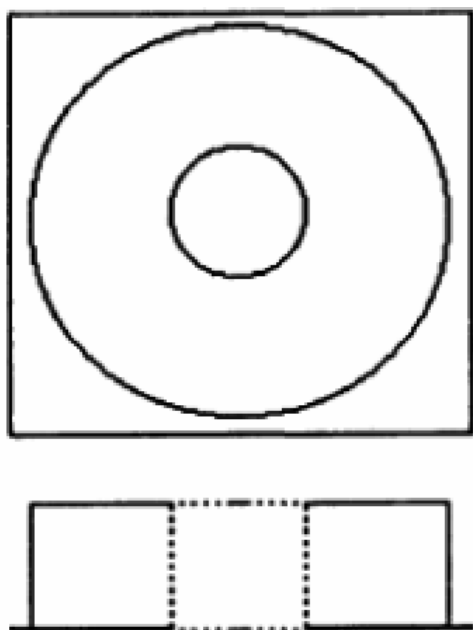


Figure 16.10 The capacitor with ground plate.

The conductor rod is threaded on both ends. The rod is slipped into its container box with the top and front cover removed and slipped through a centered hole in the back cover. A ceramic insulator is slipped on over the threads and centered in the hole of the back cover. A washer, smaller in diameter than the insulator, is slipped on with the nut. This forms the output terminal. The components are slipped on one at a time over the long exposed conductor via the open front and top of the filter container. Each capacitor is soldered before feeding on the next inductor (toroid) until all the components are installed. The front cover is then installed and soldered, followed by the ceramic insulator, and then the washer and nut. This forms the input side of the filter. The filter is then tested and cured in an oven in vacuum and then retested. Often the feedthrough capacitor requires additional torque to ensure proper ground and terminal contact. The top cover is then soldered in place. A potting compound is often used to hold the elements in place. This unit should not be required if any of the components are snug to the conductor (this assumes the rod is rigid). If they are loose, or if the specification calls for potting compound, use just enough in the bottom to hold the components in place or stationary. These units are heavy enough now without the potting compound. To keep the filter as light as possible, mix microballoons with the potting compound.

导电轴两端开有螺纹，取下壳体的顶盖和前盖，将这个轴穿入壳体中并穿过后盖中心的孔。并将陶瓷绝缘子穿在导电轴上，然后穿入直径小于陶瓷绝缘子的垫片并拧上螺母。这样就形成了输出端。在滤波器的前端，一次穿一个元件到导电轴上，在穿入下个电感（磁环）之前需要将电容焊接好。穿完了所有的元件后，就可以安装并焊接滤波器前盖了。随后安装陶瓷绝缘子、垫片和螺母。最后这些元件就形成了滤波器的输入端。接下来测试滤波器，

如果发现问题就将滤波器放到真空炉中修复，然后再进行测试。通常穿心电容需要额外的扭矩以确保可靠接地和终端可靠接触。一般会用灌注混合物的方法来固定元件，如果每个元件都紧密地贴在导电轴上（这假设轴是刚性的），那么就不需要灌封了。但如果这些元件安装的很松，或者规范要求灌封，那在滤波器底部灌封就足够能固定元件了。这些滤波器在没有灌封时就已经很重了，所以为尽量降低重量，会在灌封料中填充微小的空心球。

The advantages of filters in parallel are as follows (Figure 16.11):

- 1). The current reduction drops the silver-plated rod diameter by approximately

$$\frac{I_d}{\sqrt{N}}$$

where N is the number of filters in parallel, not the turns. This reduces the I_d , giving more inductance and capacitance for the O_d .

- 2). The inductor value becomes reasonable by being multiplied by N, and the capacitor value is divided by N, reducing the size of the capacitor. This improves the capacitor SRF and the inductor efficiency.
- 3). H is reduced to H/N, reducing the size of the gap needed, where N is the number of filters in parallel, not the number of turns. The value for turns is still equal to 1.
- 4). Lower current filters may now be conventionally designed filters in parallel rather than the type discussed here.

并联安装方式的滤波器有如下优点（图 16.11）

- 1) 电流降低导致镀银的导电轴降低为 $\frac{I_d}{\sqrt{N}}$ 。此处 N 不是匝数，而是滤波器并联个数。

此时匝数仍然等于 1。

- 2) 通过将电感的值乘以 N 倍，使得电感的值变得更加合理；把电容值缩小到原来的 1/N，这样就减小了电容的物理尺寸。结果是并联提高了电容的 SRF 和电感的功效。

- 3) H 减小到 H/N，这样就使得需要开的气隙尺寸减小了，此处 N 仍然是滤波器并联个数。匝数同样也等于 1。

- 4) 并联使用的低负载电流的滤波器是常规设计的滤波器，而不是此处讨论的滤波器类型。

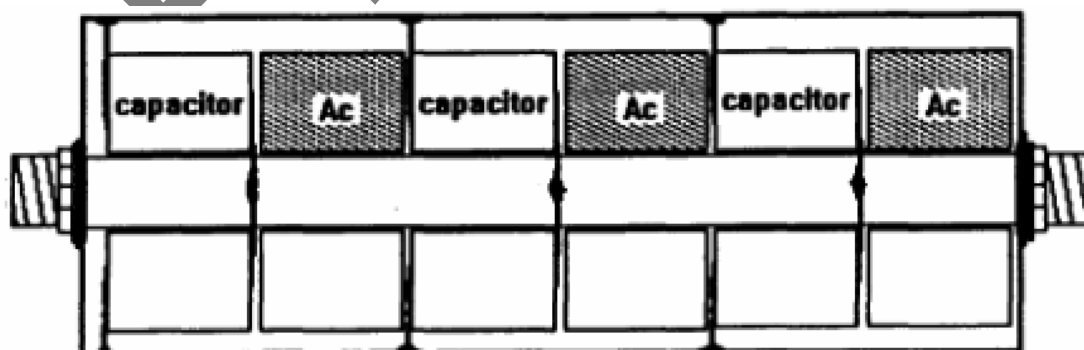


Figure 16.11 Top view of high-current filter showing three sections.

The equation for the inductor width, repeated here, is
此处再次给出电感宽度的表达式

$$W_l = \frac{4.043Lg10^8}{O_d S_f} = \frac{404.3gL_{uh}}{O_d S_f} \quad (16.17)$$

This is the initial full-sized filter, before paralleling. The value of the paralleled inductance is equal to the individual inductor of Equation (16.17) times N, the number in parallel.

(16.17) 式表示的是没有进行并联设计的最初的滤波器的尺寸。并联电感等于 (16.17) 式中单个电感的 N 倍，同样 N 为滤波器并联个数。

$$W_{ln} = \frac{404.3NgL_{mh}}{O_d S_f} \quad (16.18)$$

Returning to the initial full-sized filter, before paralleling, the value of paralleled capacitance, then, is equal to the individual capacitor divided by N. This is the capacitor width divided by N:

同样，并联设计下的电容值等于没有进行并联设计的最初电容值的 1/N。这样并联设计后的电容宽度为最初电容宽度的 1/N：

$$A_w = \frac{4CKTt}{p(D_s^2 - D_a^2)} \quad R = \frac{4CKTt}{p} \quad W_{cn} = \frac{R}{N(O_d^2 - I_d^2)} \quad (16.19)$$

A_w is the full capacitor width, so this is again the initial value of the capacitor, before paralleling the filters. This means that W_c is A_w divided by N. The total length of the filter-back cover to front cover, approximately-is

A_w 是最初的电容宽度。这就意味着 W_c 为 A_w 的 1/N。因此滤波器从后盖到前盖的总长度近似为

$$W_{LC} = 1.1S(W_{cn} + W_{ln}) = 1.1S \left[\frac{R}{N(O_d^2 - I_d^2)} + \frac{404.3gNL_{mh}}{O_d S_f} \right] \quad (16.20)$$

where S is the number of filter elements (the number of L filters in tandem here-six) and N is the number of filters in parallel. The multiplier, 1.1, is a factor allowing for the margins, capacitor lead thickness, the shield-if used-and for soldering. R is found from the initial capacitance needed, in uF, before paralleling. L_{uh} is the inductance in uH before paralleling. The inductance and capacitance were determined initially from the number of filter elements in tandem S. S must be an even number for those folded back and, even or odd, for those straight in line. The volume for the full filter, including all those in parallel, is the full filter length W_{LC} , from Equation (16.21), times the O_d^2 multiplied by the number of filters in parallel N.

此处 S 为滤波器元件数（此处的前后层叠 L 型滤波器的元件个数为 6）且 N 为滤波器并联数。乘数 1.1 是考虑了余量、电容引线厚的、焊接用屏蔽物等因素后的因子。R 为并联前最初电容所需要的数值，单位为 uF。 L_{uh} 为并联前的电感。电感和电容值最初是由滤波器

的前后层叠的元件个数 S 决定的。另外，对于折叠型的滤波器 S 必须为偶数，而直线型 S 可以是奇数或偶数。整个滤波器的体积（包括所有并联的滤波器）为滤波器长度（由式 (16.21) 得到的）与 O_d^2 的积再乘以滤波器并联数 N 。

$$V_{tot} = W_{LC} N O_d^2 = 1.1S \left[\frac{R}{N(O_d^2 - I_d^2)} + \frac{404.3gNL_{mH}}{O_d S_f} \right] N O_d^2 \quad (16.21)$$

If O_d is, again, $\gg I_d$, the denominator of the first term cancels, reducing the first term to R . The second term is directly multiplied by $N O_d^2$:

如果 $O_d \gg I_d$ 则分母的第一项可以化简为 R ，并把第二项直接乘以 $N O_d^2$ ，得：

$$V_{tot} = 1.1S \left(R + \frac{404.3gN^2 O_d L_{mH}}{S_f} \right) \quad (16.22)$$

Whatever the method, this volume remains the same for all the different numbers in parallel. Choose a combination that gives the filter a nice form, in which the filter is not a cube or 60 feet long, 4 inches wide, and 8 inches deep. Filters can be folded back on themselves, dividing the length by 2 and twice the depth. Figure 16.12 is a nice form in which the length is twice the diagonal.

无论采用什么方法，即使采用不同数目的滤波器并联设计，其总体积也并不发生变化。当然设计上需要选一种好的组合形式，这样可以将滤波器的形态设计的比较好（滤波器不再是立方体，或者是如 60 英尺长、4 英寸宽 8 英寸深这样的尺寸）。滤波器也可以采用折叠设计，这样可以将滤波器长度减半而把深度加倍。图 16.12 就是一种较好的滤波器形态，它的长度是对角线的两倍。

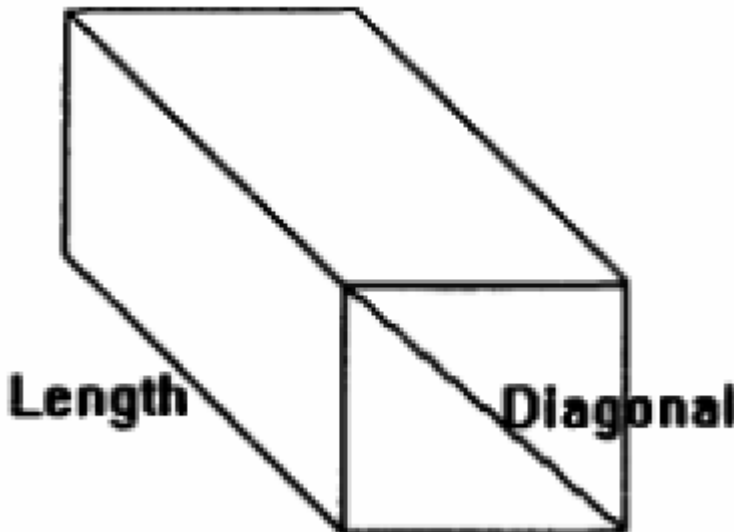


Figure 16.12 Ratio of diagonal to length.

The easiest method is to calculate the diagonal of the end piece compared with

the length. Twice the diagonal is normal and about the minimum, three times the diagonal is about maximum. There are three equations. The first equation is for straight where the O_d is the depth with N multiplied by O_d for the width. The second shape has the same width but the length is half and the depth is twice as large, or twice the O_d . This is folded back, so that the input and output terminals are on the same face (see Figures 16.13 and 16.14). The last is the even count type, such as 4, 6, 8, and 9, which gives 2×2 , 3×2 , and 4×2 , which requires the full length, and the width and depth are multiples of as be of O_d as before. These equations cannot be differentiated to solve for a minimum because all I have tried give points of inflection.

最早使用的方法是：将最终滤波器样品设计为长度最小约为对角线的两倍，最大约为 3 倍。此处有 3 个等式。第一个等式表示的是直线型滤波器，其中 O_d 为深度， N 乘 O_d 为宽度。第二种形状具有相同的宽度，但是长度减半而深度为 O_d 的两倍。这种滤波器类型为折叠型，所以滤波器的输入和输出端子都处在同一个面上（参见图 16.13 和图 16.14）。最后一种为偶数型，如需要的滤波器长度、宽度和深度为 2×2 、 3×2 和 4×2 ，倍于 O_d 。通过这些等式并不能得出最小值，这是因为在此处我只是使用这些公式来表明滤波器可以变形的观点。

The three equations for the length to equal twice the diagonal follow the assumption that $O_d \gg l_d$. Any other ratios for the equations are easily established. Again, watch for higher l_d dimensions because other materials require a higher cross-sectional area than copper so that the O_d may not be all that much greater than the l_d :

这三个表达式都是滤波器长度等于对角线二倍，其假设条件是 $O_d > l_d$ 。而其它长度与对角线比例关系的等式同样会很容易推导。但需要注意 l_d 的尺寸，这是因为如果用其它材料制作滤波器其截面积会大于使用铜来制作，因此 O_d 并不都会远大于 l_d ：

$$\begin{aligned} 1.1S \left[\frac{R}{N(O_d^2 - I_d^2)} + \frac{404.3gN^2O_dL_{mH}}{S_f} \right] &= 2O_d^3N\sqrt{N^2 + 1} \\ 0.55S \left[\frac{R}{N(O_d^2 - I_d^2)} + \frac{404.3gN^2O_dL_{mH}}{S_f} \right] &= 2O_d^3N\sqrt{N^2 + 4} \\ 1.1S \left[\frac{R}{N(O_d^2 - I_d^2)} + \frac{404.3gN^2O_dL_{mH}}{S_f} \right] &= O_d^3N\sqrt{N^2 + 16} \end{aligned} \quad (16.23)$$

The first equation is for one filter deep, or depth O_d and N multiplied by the O_d wide. The second equation is for the folded-back type, so the depth is again twice the O_d , the width is still N multiplied by the O_d , and the length is half. The last is for the even count 4, 6, 8, and 9. Again, parallel filters are rarely more than six. Surely by this count conventional filter design could handle this reduced current. Here, four in parallel would give 100A each for the case listed in Table 16.3, and a conventional filter could handle this current. These form

cubic equations. For a current of 400A, the parameters are as listed in Table 16.3 for filters in parallel. Each listing is for one through nine filters in parallel. Rarely are more than four in parallel ever used.

第一个等式只是表示一个滤波器的深度或深度 O_d 和 N 乘以 O_d 得到的宽度。第二个等式表示的是折叠型滤波器，所以深度仍是 O_d 的二倍，而长度减半。最后一个等式是表示 4、6、8 和 9 的偶数型滤波器。通常并联滤波器的数目很少大于 6。这个数量的常规滤波器并联会确保滤波器能承载因并联后而减小的电流。此处表 16.3 列出的壳体的滤波器，4 个并联且每个能承载 100A 电流，每个滤波器都采用常规的设计就能承载此电流。这些滤波器形成了立方体结构。对于 400A 电流，并联滤波器的参数列在表 16.3 中。每个列表都含有 1~9 个滤波器并联的情况，但是实际上很少有多于 4 个滤波器并联的情况。

Table 16.3 One to Nine Filters in Parallel

Z	S	F_o	L	C	I_{rms}	dIA	Width
1.1	6	4400	39	32.8	400	11.5	32.5
2.2	6	4475	78	16.2	200	8.0	35.8
3.3	6	4530	115	10.6	133	6.4	40.0
4.4	5	3850	181	9.4	100	5.8	52.7
5.5	5	3900	224	7.4	80	4.9	57.5
6.6	5	3900	269	6.2	66.6	4.4	62.0
7.7	5	3930	311	5.3	57.2	4.0	66.3
8.8	5	3930	356	4.6	50	3.6	70.3
9.9	5	3960	397	4.0	44.5	3.4	74.1

The single filter giving an impedance of 1.1Ω is ridiculous. Look at the diameter of the inductors and capacitors. I am not sure that the capacitor can be wound, because most extended foil winding machines can handle about 6 inch diameters. The inductor can be as large as 3 feet in diameter and the same width at National-Arnold in Adelanto, California. The volume is good, and so is the width (this should now be length). Two in parallel, giving 2.2Ω each, is better, giving a smaller diameter and less width. All the filters in Table 16.3 are O_d depth element and N multiplied by O_d wide.

把单个滤波器阻抗设计为 1.1Ω 是十分荒谬的。查看一下电感和电容的直径会发现，并不能确定一定能绕制出此电容。这是因为多数延伸箔绕制机只能绕制大约 6 英寸的直径。National-Arnold in Adelanto, California 的电感可以制作大到 3 英寸的直径和宽度，这个体积和宽度（现在应称作长度）是比较适合实际使用的。在两个滤波器并联的情况下，则需要每个滤波器阻抗为 2.2Ω ，这样直径和宽度都比单个滤波器的设计值小些。表 16.3 中所有参数都是深度 O_d 和 N 乘以 O_d 得到的宽度。

Figure 16.13 and 16.14 show the folded-back type.

图 16.13 和 16.14 表示的是折叠型滤波器。

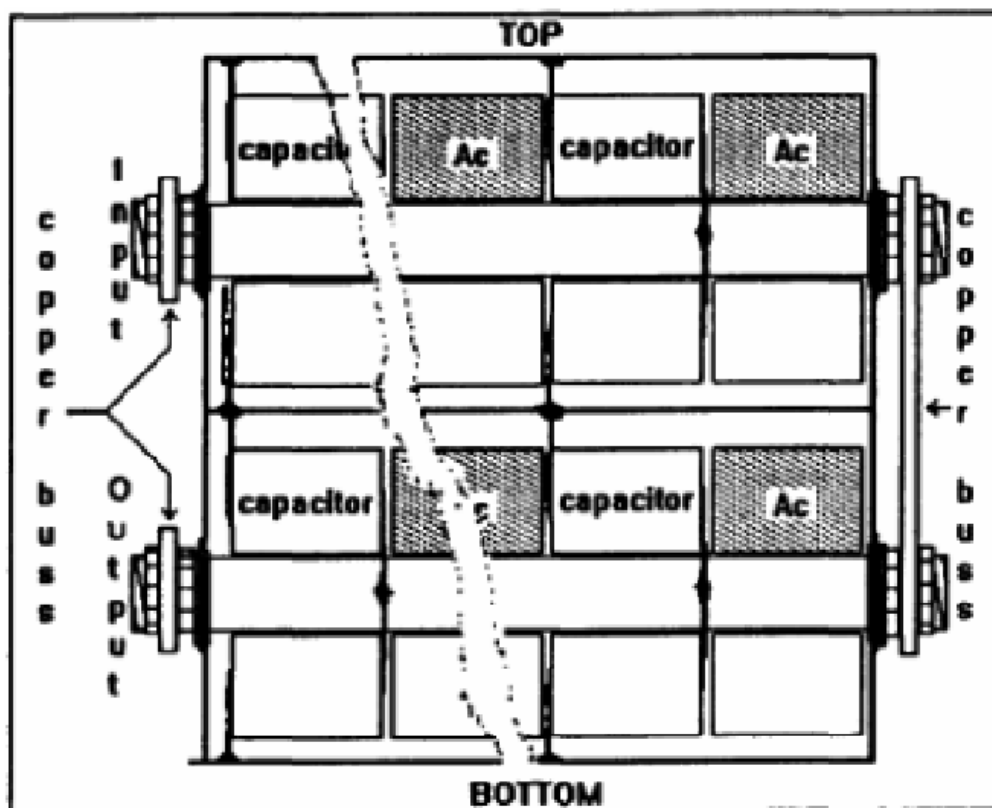
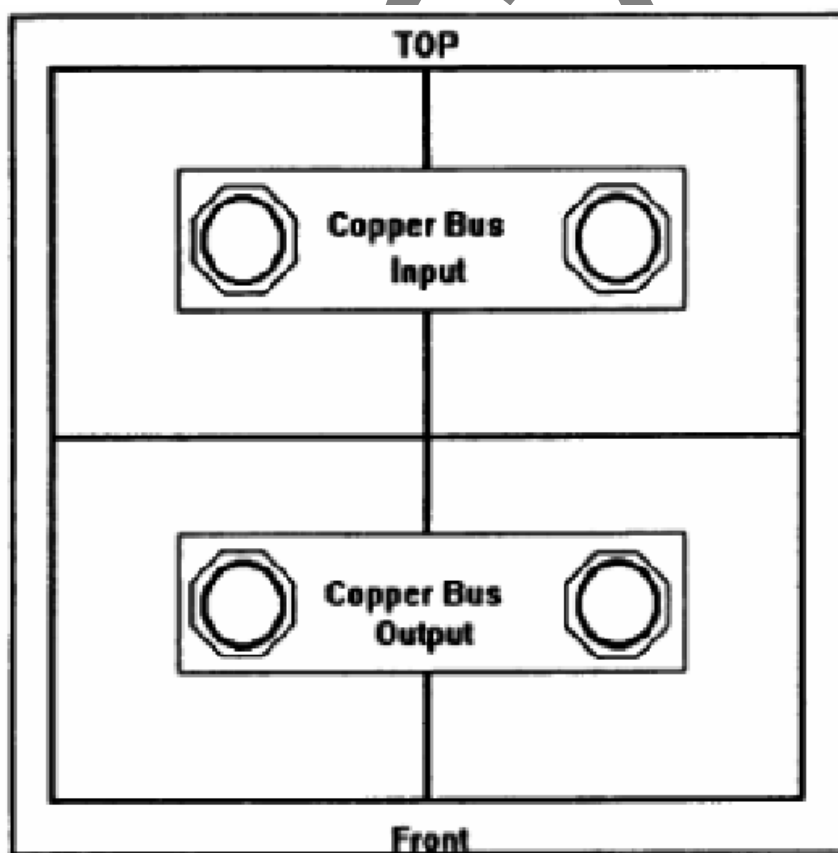


Figure 16.13 The side view of two filters in parallel folded back.



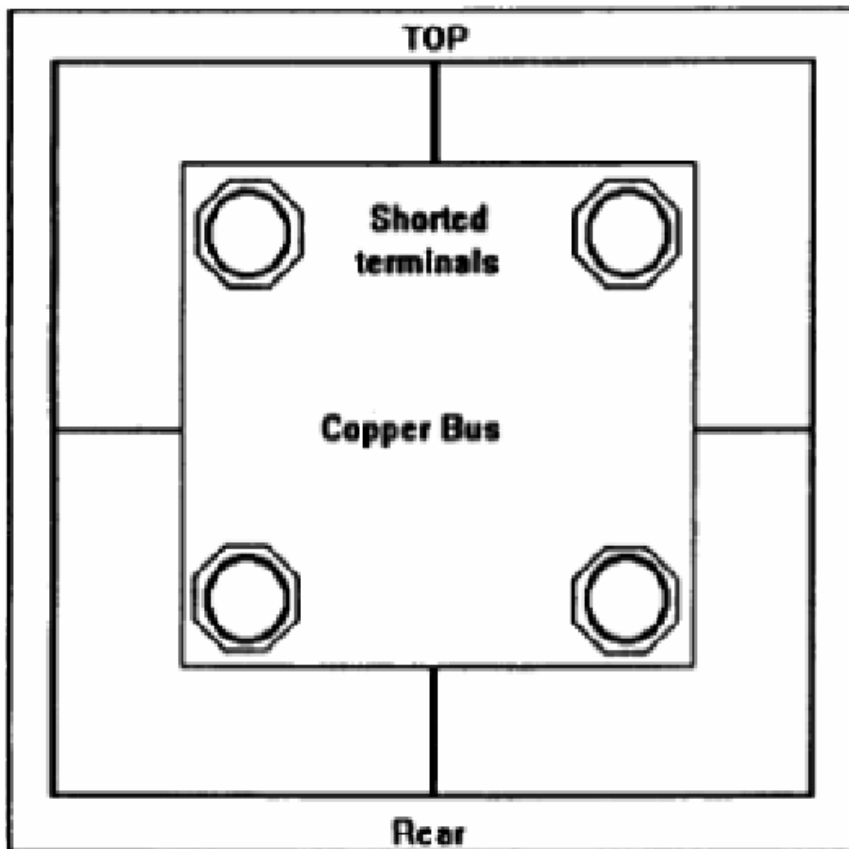


Figure 16.14 Front of two filters in parallel folded back with rear view (below).

The rear terminals are all shorted together, and the metal protective shroud that normally covers the entire rear is not shown. In the front a division is shown between the top and bottom halves. The same idea is used in designs with three, five, and seven (rarely used) filters. These are all folded back, as in these figures. The number of stages S must be even to split between the top and bottom half of the two folded-back designs. The length is cut in half (plus some for the shrouds covering both the front and rear connections). Four is a two by two, six is a three by two, and eight is a four by two, requiring the full length. Nine is a three by three, also running the full distance. The approximate sizes for the five folded-back designs is listed here. Again, long before these many filters are in parallel, the design can revert to conventional filter types.

每个单元的后部的终端都短接在一起，通常会有一个金属保护盖安装在后部，这样就看不到后部终端短接的情况了。在前部，分为上下两个半区。同样对于 3、5、7 个（很少使用）滤波器并联的设计方法是一样的。如图，这些滤波器都是折叠型的。对于折一次的折叠型，节数一定要是偶数，这样可以在前端面拆分成对等的两半。此时滤波器的长度减半（但需要增加前后保护盖的尺寸）。对于 4 节则分成 2×2 个，6 节分成 3×2 个，8 个为 4×2 个，9 个为 3×3 个，这些单元长度相加就是滤波器的整体长度。在此处我列出了 5 个折叠型滤波器的设计数据。同样，这种多个滤波器并联的设计方案使得每个滤波器都可以采用常规滤波器类型。

The five in parallel and folded back for 400A (now 80): $R=601.38$ and

$Q=0.3558$ with each inductor $=195\mu\text{H}$. Each capacitor $=6.6\mu\text{F}$. The required diameter $=4.3$ inches. $F_0=4436$ (very good). The folded length is approximately 28.2 inches. $Z=5.5$, $s=6$ (even so, the bottom and top half component counts are equal), and the volume $=2.9$ feet³.

对于 400A 电流的需求, 五个折叠型滤波器并联设计为: $R=601.38$ 和 $Q=0.3558$, 每个电感 inductor $=195\mu\text{H}$, 每个电容 $=6.6\mu\text{F}$ 。滤波器需要的直径 $=4.3$ inches。 $F_0=4436$ (非常理想)。折叠的长度近似为 28.2 inches。 $Z=5.5$, $s=6$ (虽然如此, 但上半部和下半部的滤波器元件数还要是相等的), 体积 $=2.9$ feet³。

Granted, this is only an approximation, but if a 400A filter can be built in less than 3 feet³, this is very good. The inductors would be 1.8 inches wide, and the capacitors would be 6.5 inches wide. The capacitors may have to be split, requiring 3.27 inches. Winding machine can handle various sizes. Extra room is allowed for soldering, width of contacts, and margins. It should be realized that the use of more than four in parallel is rare, but these are shown here for comparison. Also, the filter design can revert to conventional design techniques with this lower current of only 80 A. This high-current design really starts at 100 A or so, depending on the line voltage.

当然这只是近似, 但是如果一个 400A 额定电流的滤波器体积可以小于 3 立方英尺, 这就是非常好的一种情况。这时电感宽度为 1.8 英寸, 电容宽度为 6.5 英寸。但电容可以拆分, 所以只需要 3.27 英寸宽。电容缠绕机可以缠绕这种尺寸的电容。当然考虑焊接、连接端子和裕量等因素还需要留出余量。还有一点需要明确, 目前很少使用超过 4 个滤波器并联的设计, 所以此处给出列表只是为了作对比使用。另外, 如果额定电流只有 80A 那么滤波器设计就可以使用常规设计, 高电流的设计方案的起始电流数值应为 100A (也与线电压相关)。

The same technique can be used on rectangular buses using C cores of the same material instead of toroids. The capacitors must be wound on a special rectangular arbor and thus require more care while winding. Often the dielectric is composed entirely, or partly, of reconstituted mica because of the abrupt turns required for Mylar. This overstresses some of the dielectrics.

对于使用 C 型磁芯来替代圆磁环的方形总线设计也可以采用同样的设计技术。电容要缠绕在一个特殊的方形轴上, 这需要缠绕时更仔细些。电容的介质常常采用再生的云母, 这是因为 Mylar 电容所需要的生硬的缠绕方式, 这种过应力会限制一些介质的使用。

The strap in Figure 16.15 is stainless steel, not strap iron, as a designer once used years ago after the last of his stainless steel had been used. The strap iron carried almost all of the flux around the two gaps and melted in a few seconds. These cores are also available from National-Arnold.

图 16.15 中的捆带是由不锈钢制成而不是铁带。几年前铁带在不锈钢带使用前一度曾被使用。铁带会承载两个气隙的几乎所有的磁通, 会在很短时间因为过热而融化。另外, 这些磁芯可从 National-Arnold 公司购买。

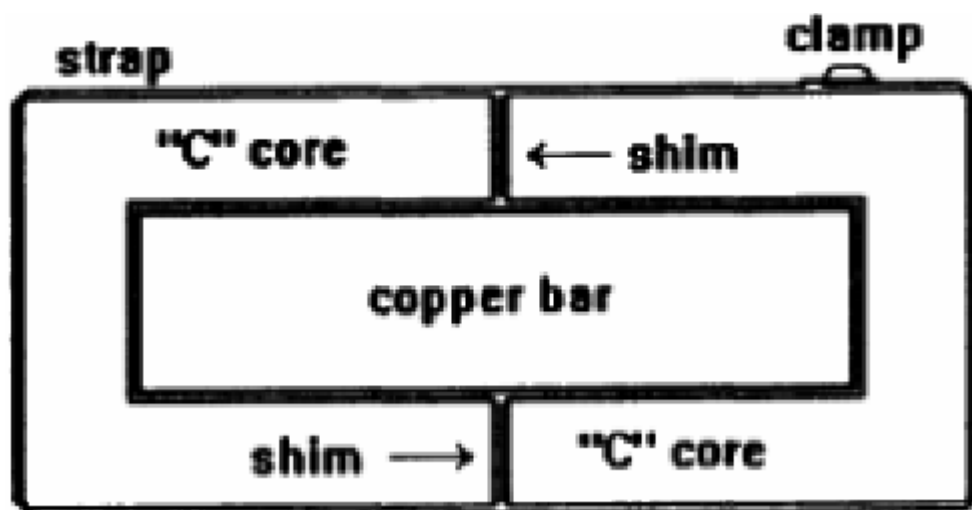


Figure 16.15 The C core showing shims and clamp.

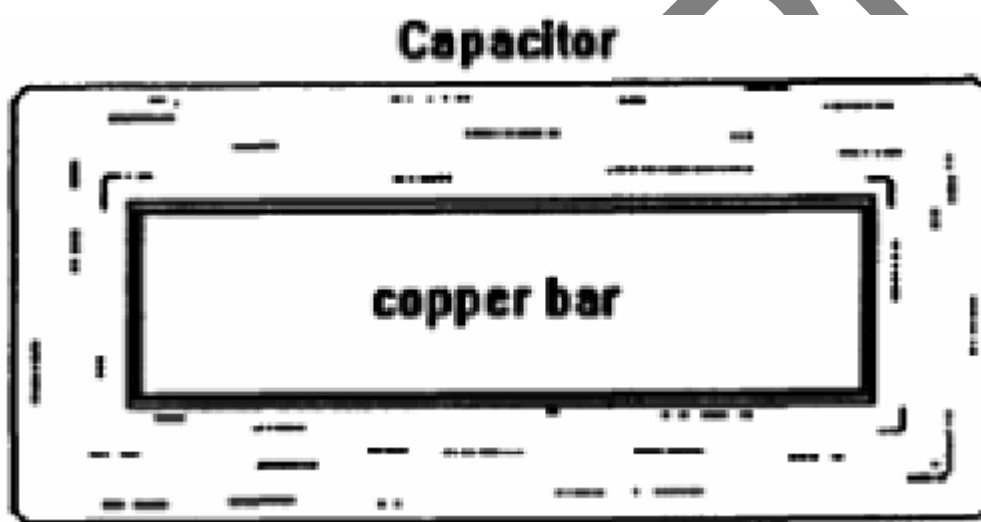


Figure 16.16 The square capacitor used for copper bar.

Mount the capacitor the same way as in Figure 16.16 with either a shield or leads. This design technique is summarized in Section 16.3.

按图 16.16 的方法安装电容 (或安装在屏蔽导体面上、或为引线式)。这种设计技术在 16.3 节会有一个概括性的介绍。

§16.2 High-current Second Method

§16.2 大电流设计的第二种方法

Each inductor assembly (C core) surrounds the bus, and each capacitor assembly has its own rod, or bus, and these are tied together at the main bus (Figure 16.17).

这种方法是：每个电感 (C 型磁芯) 围绕总线装配，而每个电容自己都有一个穿心轴杆，并且在总线上连接在一起 (图见 16.14)。

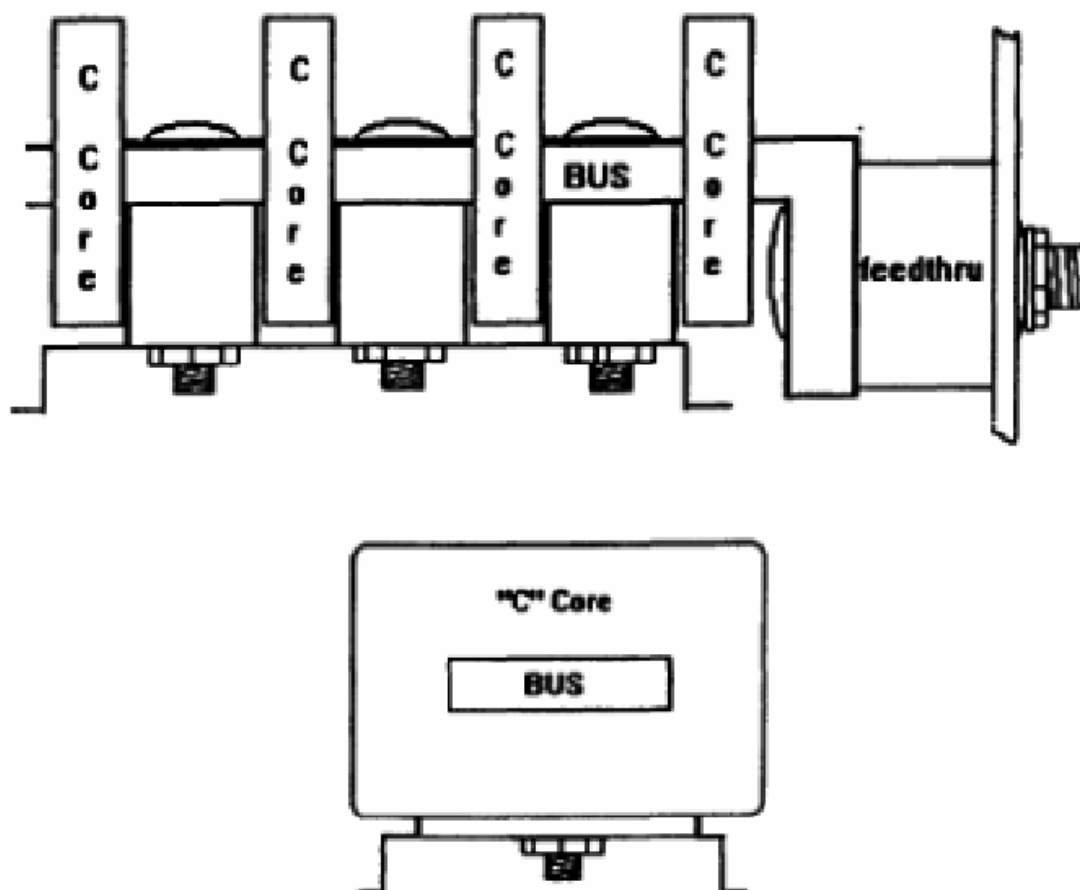


Figure 16.17 Second method for the high-current design.

The three capacitors are the feedthrough type, but the bolt carries no current as the normal feedthrough would and as the bottom feedthrough capacitor in Figure 16.17 would. The capacitors carry only the normal capacitor "leakage current"—really reactance current to ground—but this is not through the bolt. These three feedthrough capacitor bolts are "hot." The plate to which the feedthroughs are bolted is grounded, and the bolt is isolated from the plate. The three capacitor foils are pressed to the ground plate, giving good SRF, equivalent series inductance (ESL), and resistance (ESR). The extra ground plate can be avoided if these three bolts are nonconductive and do not need to be isolated from the plate or the outside filter wall. The nonconducting bolts, here, would protrude through the wall of the filter and could be touched without shocking. The advantage of this style over the style using the ground plate is that the three capacitors, along with the last feedthrough, could be torqued again, after the heat cure, from outside the filter body. In the first style, the cover over these three bolts must be left off through the heat cure to have access to these bolts. This torque is required for proper pressure for both capacitor foils of each capacitor to function properly. There are several advantages of this style over the type in Section 16.1:

图 16.17 中的三个电容都是穿心型的，但是此穿心电容的芯轴不像常规穿心电容那样是载流的。这些电容承载的是电容的漏电流，这个漏电流是纯粹的对地电抗的电流，而漏电流

并不通过芯轴。这三个穿心电容的芯轴是与电源线同电压的，而安装穿心电容的平面是接地的，其芯轴是与此平面绝缘的。这三个穿心电容的带金属箔的侧面压接在地平面上，因此会有较佳的 SRF、ESL 和 ESR。如果电容的芯轴是不导电的，那么就不需要为使芯轴与此平面或滤波器外壳之间绝缘而进行特殊的地设计。此处这个不导电的芯轴会穿过滤波器外壳并突出来，即使接触到也不会产生电击。这种类型的设计比使用地平面的设计类型优越的地方是：这三个电容器以及最后的那个穿心电容（图 16.17 中的第四个电容）在滤波器被加热后，可以在滤波器外部重新将这些因热胀冷缩而松动的电容拧紧。而采用第一种设计类型，则需要拆下壳盖来拧紧固定电容的螺母。当然这个扭矩要适宜，以便电容能正常实现功能。这种设计与 16.1 节的设计相比有以下几个优点：

1. In the first style, the I_d of all the capacitors had to be the same as the inductors. In the second style, the I_d can be very small for the three capacitors to ground. This is not true of the output feedthrough capacitor. This output capacitor bolt carries the full filter current to the outside world. The bolts through the capacitors to ground carry no current (unless it is conductive and shorted) to the outside world. The output feedthrough capacitor bolt must be able to carry the full load current to the outside world, but this is a much smaller capacitor value.

1. 对于第一种类型，所有电容的 I_d 都必须与电感的相同。而在第二种类型中，对于那三个对地电容，其 I_d 可以很小。但对于（见图 16.17）输出处的穿心电容则与电感的 I_d 要相同。而且这个电容的芯轴还要承载整个滤波器承载的电流。对地的那三个电容的芯轴不承载电流（除非芯轴是导电的且被短路）。并且输出侧的穿心电容的容值很小。

2. The opposite is true of the inductor. The bus can be as large as needed to carry the full filter current through the center of the C core, because this second style, the inductor bus, does not pass through the I_d of the capacitor.

2. 对于电感则与电容情况相反。因为在第二中类型设计中，电感的总线可以不考虑电容的安装，而是可以按滤波器需要的载流量来增大尺寸，只要能穿过 C 型磁芯就可以了。

3. In the second style it is easier to adjust the tension required for proper capacitor action.

3. 第二种设计方法使得调整电容的松紧变得比较容易，这样可以使电容正常工作。

All the methods that can be developed to design these high-current filters require iterations. As the O_d grows, with inductance and capacitance values held constant for the proper design, the width of the capacitor decreases. This increase in the value of O_d increases the M_{pl} , which decreases the H —the MMF—which moves the flux density away from saturation—and increases the A_c value of the inductance. If A_c and M_{pl} grow at the same rate, this holds the inductance constant. This increase in M_{pl} , however, requires a larger gap to hold U_e constant; otherwise, the inductance increases. So, around and around it goes. The disadvantage is that the bus must be oversized to allow room for the capacitor feed. A copper bus is not very big to handle the current—400 A here. Although copper can be used here because no torque is required, often poorer

conductors with very conservative current densities are used. This gives the width needed to support the capacitors to ground but also increases the filter volume. This is a trade-off. C_m is the circular mils per ampere required, and W_a is equal to FG of the C core:

所有的大电流滤波器的设计方法都可以通过重复设计的方式来改善。对于一个比较适当的设计，当 O_d 增大而电容和电感的数值保持常数时，电容的宽度会减小。而 O_d 值的增大会使得 M_{pl} 随之增大， M_{pl} 的增加会降低 H ，进一步会降低导致磁环饱和的磁通密度，结果会增大电感的 A_c 值。如果 A_c 和 M_{pl} 增大的比率相同，就会使电感保持常数。但是在 M_{pl} 增加时，需要开大的气隙来保持 U_e 值恒定，否则电感就会增加。此方法的缺点是总线必须为保证穿心电容的安装再增加余量，这样尺寸就会很大。而一般承载电流（此处为 400A）的铜总线尺寸都不太大。尽管因为没有扭矩的要求而可以使用铜总线，但是实际上还是常常使用导电性较差的导体，导电性差的导体就会尺寸较大，这就解决了对地电容安装的问题，但同时也增加了滤波器的体积。当然这也是一种折衷方案。 C_m 是需要的每安培的圆密耳数， W_a 等于 C 型磁芯的 FG。

$$W_a = 7.854 C_m I_{\max} 10^{-7} \text{ inch}^2$$

The question is, can the capacitor fit on the bus? A top view of the capacitor and inductor assembly along with the equations is shown in Figure 16.18. The approximate value of O_d can be calculated from Figure 16.18. This is because all the quantities are known (Figure 16.19). A_w should be at least the C core dimension E. The O_d should be, at maximum, the C core dimension G. If thin shims or washers are added to the bus end of the capacitor, the O_d can extend beyond the length of G to a maximum of G plus twice E. If the O_d of the capacitor is greater than this, the volume of the filter increases some.

问题是电容能安装在总线上么？图 16.18 表示的是电容和电感装配在一起的俯视图，并在图中附带了公式。 O_d 的近似值可以通过图 16.18 中的公式计算，这是因为式中所有的数值都是已知的（图 16.19）。 A_w 至少应为 C 型磁芯的尺寸 E（参见图示），最大应为 C 型磁芯的尺寸 G。如果在电容的总线终端加入薄垫片，那么 O_d 长度就会延伸到 G 和 $G+2E$ 之间。如果电容的 O_d 大于此值，那么滤波器的体积就需要增加一些。

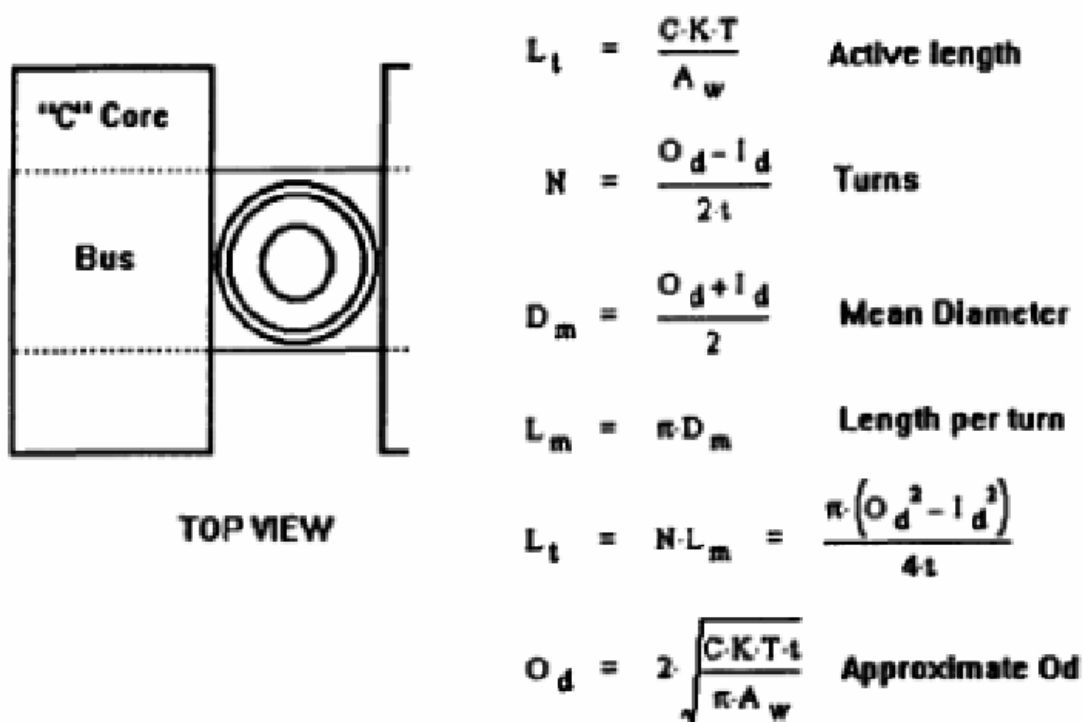


Figure 16.18 Top view of C core, bus, and capacitor with equations.

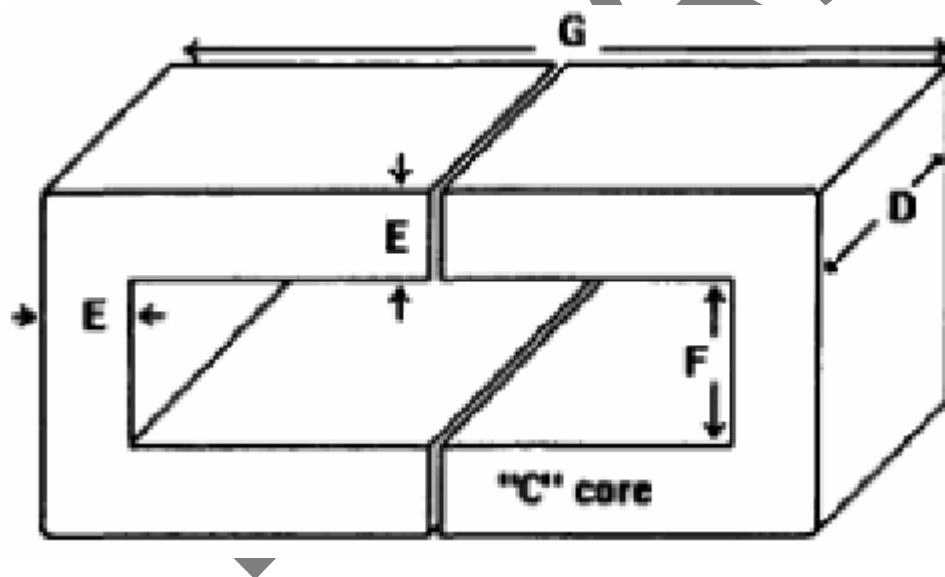


Figure 16.19 C core with dimensions.

For the inductor, the D dimension can be calculated from the equations just listed and knowing the gap, M_{pl} , A_c , and W_a , three of which are listed here:

对于电感器来讲，尺寸 D 可以通过列出的等式和已知的气隙、 M_{pl} 、 A_c 和 W_a 等值来计算。

$$A_c = 6.452 E D S_f$$

$$M_{pl} = 5.08 (G + F + 2E)$$

$$W_a = 6.452FG$$

$$A_p = W_a A_c = 41.62EDFGS_f$$

where D, E, F, and G are in inches and A_c , M_{pl} , W_a , and A_p are in centimeters. Knowing the value of the inductor, the needed width D can be found. The core manufacturer can make these cores to the needed width D, or several cores can be stacked to reach this dimension. If the capacitor O_d dimension is less than G, the capacitors can be paralleled (Figure 16.20).

此处 D、E、F 和 G 的单位是英寸而 A_c 、 M_{pl} 、 W_a 和 A_p 的单位是厘米。如果已知电感值，那么其所需的宽度 D 也就确定下来了。磁环厂家可以按需要的宽度 D 来制作磁芯，也可以通过几个磁芯叠加来达到需要的尺寸。如果电容的尺寸 O_d 小于 G，那么此电容就可以并联了（具体见图 16.20）。

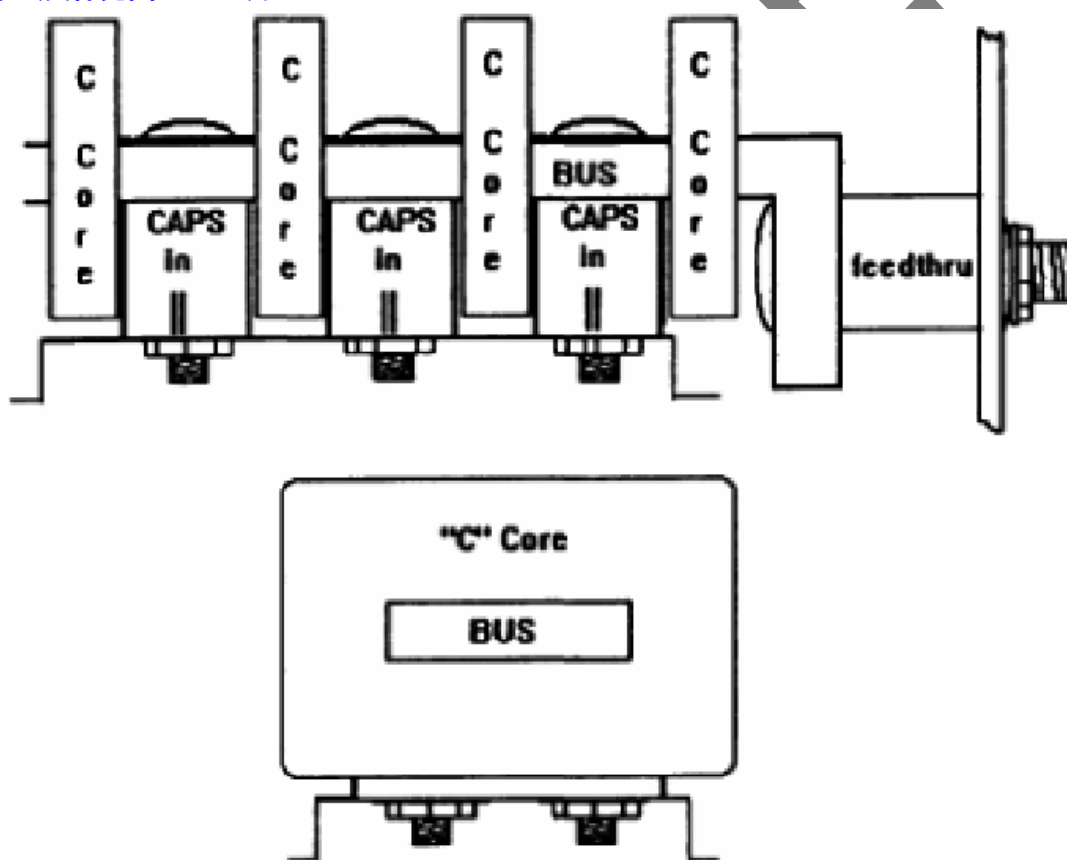


Figure 16.20 Second method showing capacitors in parallel.

The advantage of this technique is that the capacitors can be paralleled across the bus (Figures 16.21 through 16.23). This reduces the volume required for the capacitors, bringing the C cores closer together and reducing the volume of the filter. The bus area of the cross section is constant for the current required to be handled by the bus bar, so that as the width increase for the parallel capacitors, the thickness drops. There is a limit to this: the bus must fill the C core window area W_a . Therefore, there is maximum ratio of width to thickness, which is limited to about 5:1. Other wise, the C core cannot be manufactured.

The cross-sectional area is a constant that varies with the current the bus must carry. This main bus can be copper because the bus is not threaded and is not torqued as in the first method.

此设计方法的优点是，电容可以并联在总线上（见图 16.21 到 16.23）。这就减少了对电容体积的要求，使得 C 型磁环彼此接近，并最终减小了滤波器的体积。因为总线需要承载的电流是确定的，那么总线的截面积就需要是常数，所以由于并联电容的缘故导致总线变宽时总线的厚度就会降低。此处有一个限制：要求总线尺寸必须能适合 C 型磁芯的窗口面积 W_a 。因此，由于此限制导致总线的宽度和厚比的最大值约为 5:1。否则，C 型磁芯的尺寸就不能满足生产要求。总线的截面积是一个随总线承载的电流而变化的常数。这个总线可以使用铜来制作，因为此总线没有像第一种设计方法那样有螺纹和扭矩的需求。

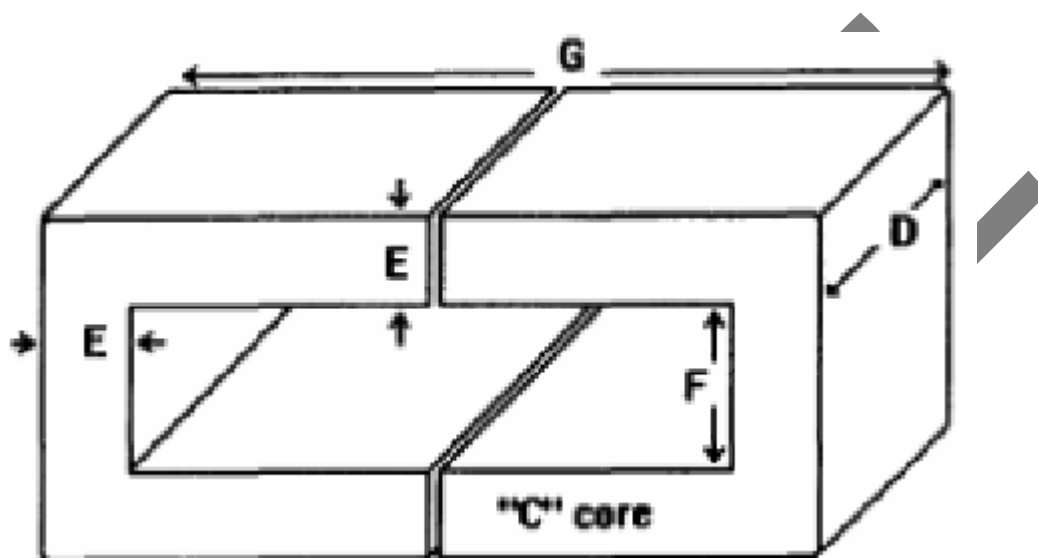


Figure 16.21 The C core with dimensions.

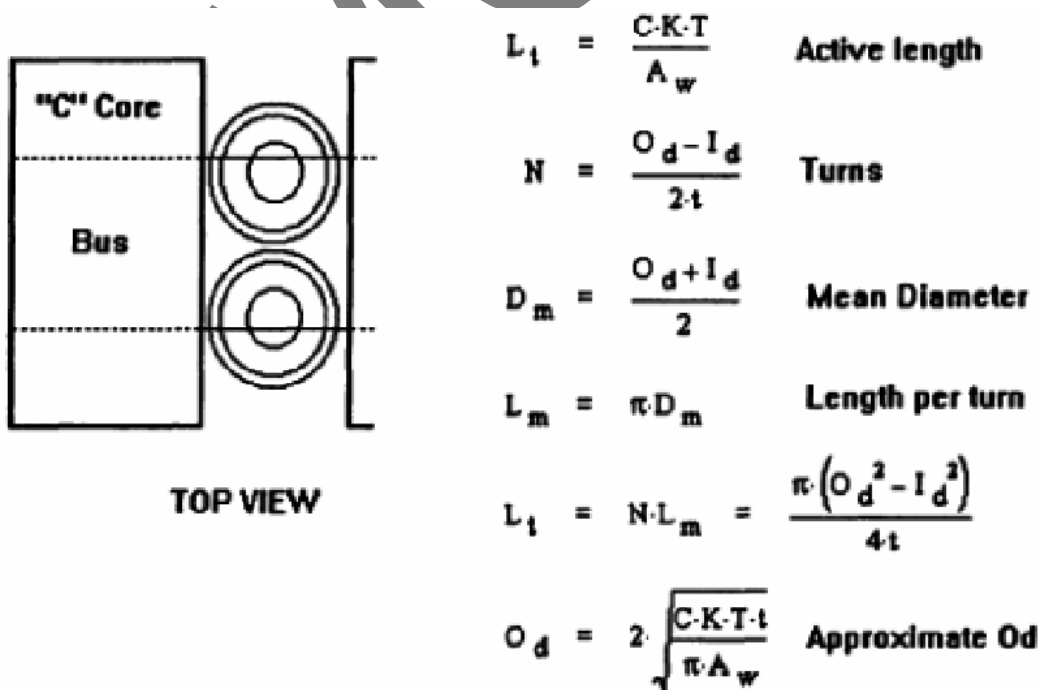


Figure 16.22 Top view of C core showing parallel capacitors and equations.

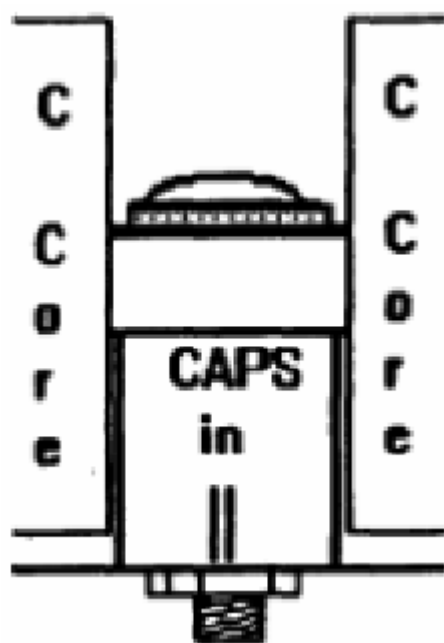


Figure 16.23 Second method for high-current filter showing added bus.

Therefore, the width of the bus is not as wide to hold more than two capacitors across the bus. Otherwise, the capacitors across the bus extend beyond the C core G dimension (window length). Also, they could extend beyond the G plus twice the E dimension ($G+2E$ =the full length of the C cores) at both edges, increasing the volume if shims or washers are added between the capacitors and the bus. (For conditions when copper must be used, some other ideas are discussed later.)

因此总线并不能宽到能容纳两个电容在一处一同并接在总线上,否则总线的宽度就会超过 C 型磁芯的尺寸 G (窗口长度)。同样,如果在电容和总线间加入垫片,那么两边也会超过 $G+2E$ ($G+2E$ =C 型磁芯的总体长度),同时也会增加滤波器的体积。(对于必须用铜总线的使用条件,其它的一些方法和思路将会在后面讨论。)

The only difference here is that C is half the value. There is also a practical limit, and keep in mind that each hole in the bus restricts the current. Sometimes thin copper busing is placed across the bus to make up for the cross-sectional area excavated for the capacitor bolts. This technique adds to the length of the bolt and is done to maintain the cross-sectional area of the bus at the point at which the bolt holes are drilled, keeping the bus temperature lower to lengthen the life of the capacitor.

此处的不同点仅在于 C 取半值。这是一个需要牢记的实际限制条件:总线上的每个孔都会限制载流值。有时薄铜总线会覆在总线上以补充安装电容的螺柱所引起的总线截面减小的现象(此螺柱挖空了部分总线)。此设计方法虽增加了安装电容的螺柱的长度,但可以补偿有穿孔处的总线的截面积,并降低总线温度延长电容寿命。

§16.3 High-Current Method 3

§16.3 大电流的第 3 种设计方法

This technique eliminates the bolt through the center I_d by using Y capacitors with very short leads. The self-resonant frequency approaches that of the feedthrough type and has little added equivalent series resistance or inductance over the feedthrough type. The advantages are as follows:

此设计方法通过使用极短引线的 Y 电容的方法，去掉了穿过 I_d 中心的螺柱。按此方法设计的电容的 SRF 与穿心型电容很接近，而其 ESR 或电感也比穿心型电容大一点。

1. Very little bus bar area is drilled out compared with the bolts in method 1 or 2.

2. The torque required for the feedthrough type of capacitor is eliminated because the capacitor is fully assembled, and stressed, before installation in the filter.

3. The leads are soldered, removing the necessary good contact to the bus bar or ground plane.

1. 与方法 1 和方法 2 相比，此方法几乎没有总线被挖空所造成的截面积减小的情况；

2. 没有穿心型电容要求的扭矩问题，这是因为电容在装到滤波器内之前已经完全安装在电路上了；

3. 引线通过焊接连接，免除了要求电容与总线和地良好接触的要求（因为焊接已经实现了良好接触——译者注）。

The disadvantage is that the capacitors can rarely be reused because of the difficulty of returning the short leads to the holes in the ground plane.

缺点是电容很少能重复利用，这是因为将短引线从地平面的孔中取出是很困难的。

The approximate equations needed to fit the capacitor are listed in Figure 16.24 and continue in Figure 16.25. A_w is the length of the capacitor in the E direction and is longer than E to keep the ground plane away from the C core inductors. The C cores are insulated, but it is still not a good idea to be pressing or touching ground. Thus, A_w is equal to E plus an 1/8 inch or longer. This eats up volume but reduces the D_x dimension. The values of C, K, T, and t are known, so L, can be solved from the equation in Figure 16.25. Remember, t is the thickness of two dielectrics and two foils in inches (see Figure 16.8)。

满足电容安装需求的近似式在图 16.24 和 16.25 中列出。 A_w 是 E 方向的电容长度，并且长度比 E 大以确保地平面与 C 型磁芯电感有效分隔。C 型磁芯虽是绝缘的，但是让它与地接触却实在不是一个好主意。因此， A_w 等于 E 加 1/8 英寸或更长的尺寸。这会消耗已有的容积，但是这样作却会减小尺寸 D_x 。如果 C、K、T 和 t 是已知的，那么 L 就可以通过图 16.25 中的等式计算出来了。记住，t 是两层介质和两层金属箔片的厚，其单位为英寸（见图 16.8）。

Also, T is the dielectric in mils. D_x can then be solved from the quadratic equation given in Figure 16.25. The last half must be smaller than the first half under the square root. This also ensures that the last half of the quadratic is smaller than the first term. The negative solution is the only valid solution;

otherwise, D_x is larger than D_y . Once D_x is known, D_a , the arbor diameter, is solved, and then O_d also follows. In Figure 16.25, the value is shown to be larger than $G+2E$ of the C core. This is okay if D_y is smaller than the container with extra clearance. Again, none of these Y capacitors should touch the container wall.

同样, T 是以 mil 为单位的介质厚度。这样 D_x 就可以通过图 16.25 给出的二次方程来计算。根号内的后半部分的值一定要小于前半部分的值, 这同样也要求最后一半的二次式小于第一项。所以负数的解是唯一有效的解, 否则 D_x 就会大于 D_y 。一旦 D_x 为已知, 芯轴的直径 D_a 就可以解出来了, 同样跟着就会得到 O_d 的解。在图 16.25 中, 此值会大于 C 型磁芯的 $G+2E$ 。如果 D_y 小于滤波器壳体的容积, 这样就可以了。同样, Y 电容不应与滤波器壳体接触。

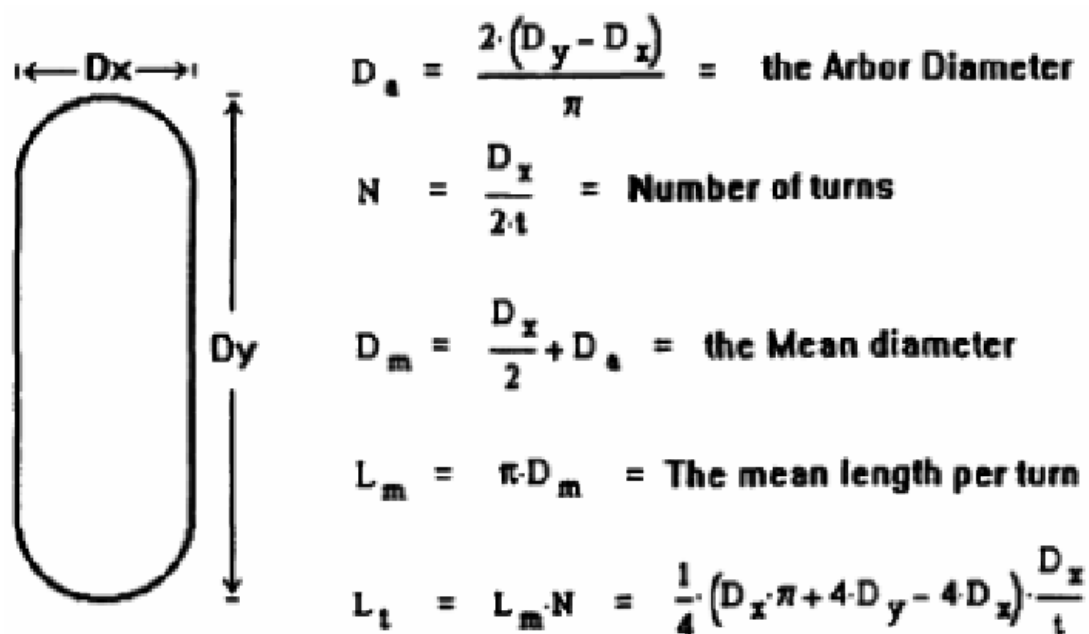


Figure 16.24 The active length L_t of pressed capacitor and equations.

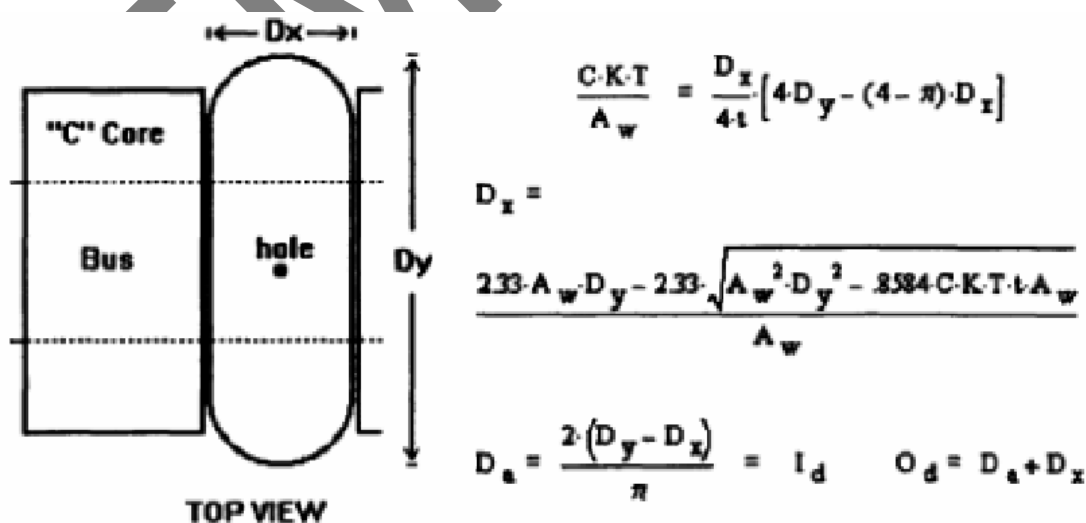


Figure 16.25 The top view of the pressed capacitor, C core, and bus with equations.

§16.4 Review of High-Current Filters

§16.4 有关大电流滤波器的回顾

Most high-current filters use pieces of these various technologies. Some extend the width of the conductor bar for the capacitor(s). Others use vee technology for the capacitors, with shunts across the vee legs to carry the main current. Others mount the inductor sideways and reverse each section so that the capacitors are on opposite ends (Figure 16.26).

多数大电流滤波器的设计会使用到这些设计方法的某些部分。一些设计方法为安装电容延展了导电总线的宽度，另外一些方法使用了通过 vee 引脚承载电流的 vee 电容设计技术，还有另外一些使用了电感在每节电路反向安装的方法，这样电容就安装在与电感相反的位置上了（图 16.26）。

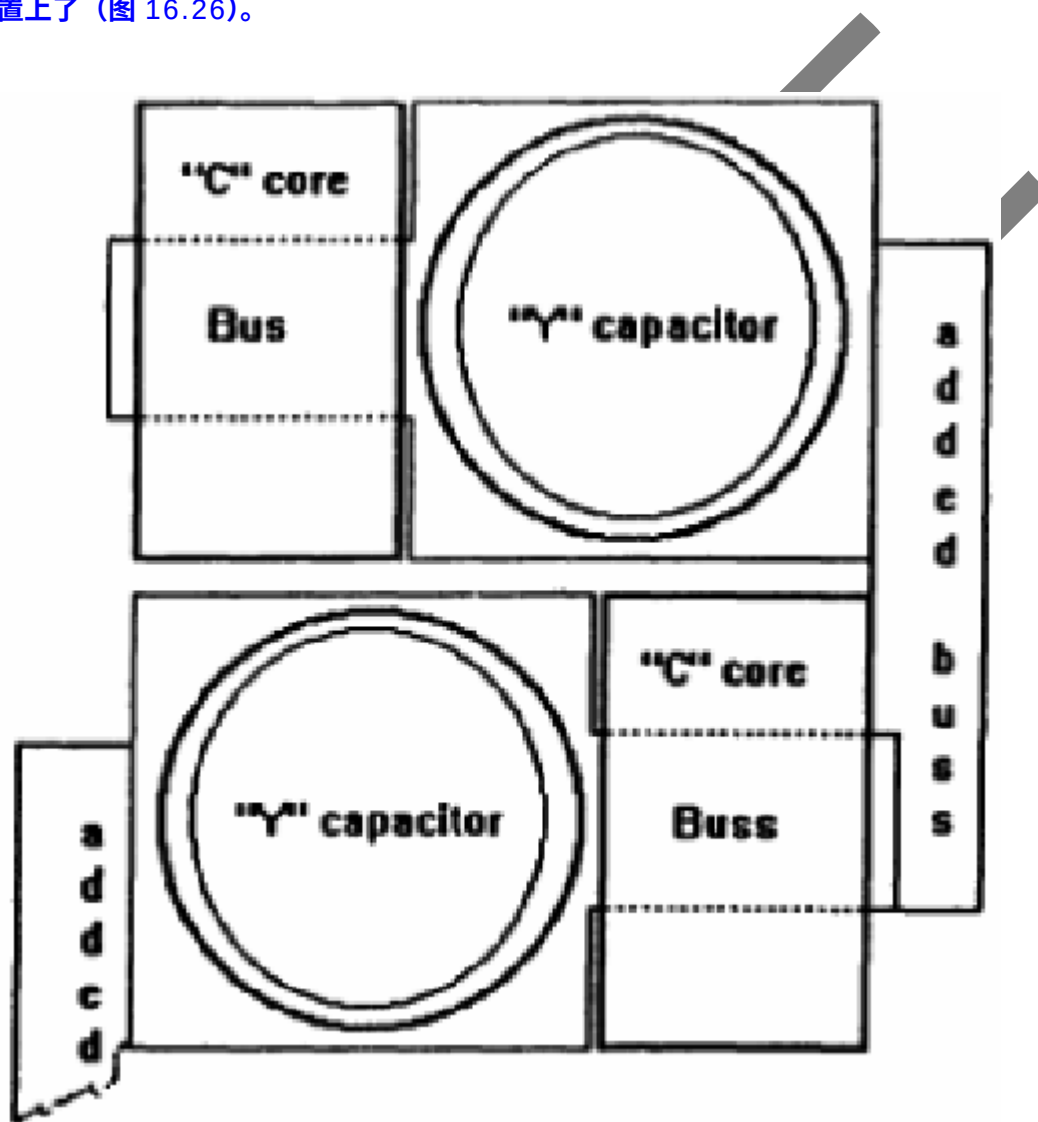


Figure 16.26 High-current filter, alternative method.

The two wires in Figure 16.27, to and from the capacitor and across the two buses, are in parallel with the single wire directly between the two buses. These wires must carry all the current between the two buses. Other wise, the diameter of the wires must increase. This is veeing the capacitor. The

inductance in both the capacitor legs adds to the inductance in the C cores if the two vee wires can handle the current. This maintains the high SRF of the capacitor. Otherwise, the shunt wire inductance is in parallel with these two vee wires (Figure 16.28). With the parallel shunt bus wire, the SRF of the vee capacitor is still higher than the situation in which the capacitor has single long lead.

图 16.27 中电容到总线和总线到电容的两条导线与一条直接连接两总线的单一导线并联。这些导线必须承载两条总线间的所有电流。如果此导线不能满足这个条件，就需要增加导线的直径。这个图表示的就是 V 型电容技术。如果 V 型电容的引脚能够承载此电流，那么引脚的电感就会与 C 型磁芯的电感相加，这样就会使电容保持较高的 SRF 值，如果 V 型电容引脚承载不了此电流，那么就需要在 V 型电容引脚间并联一条导线，这样并联导线的电感实际上就与 V 型电容并联了（图 16.28）。即使采用了并联导线的方法，V 型电容的 SRF 还是要高于电容只有一条长引脚的情况。

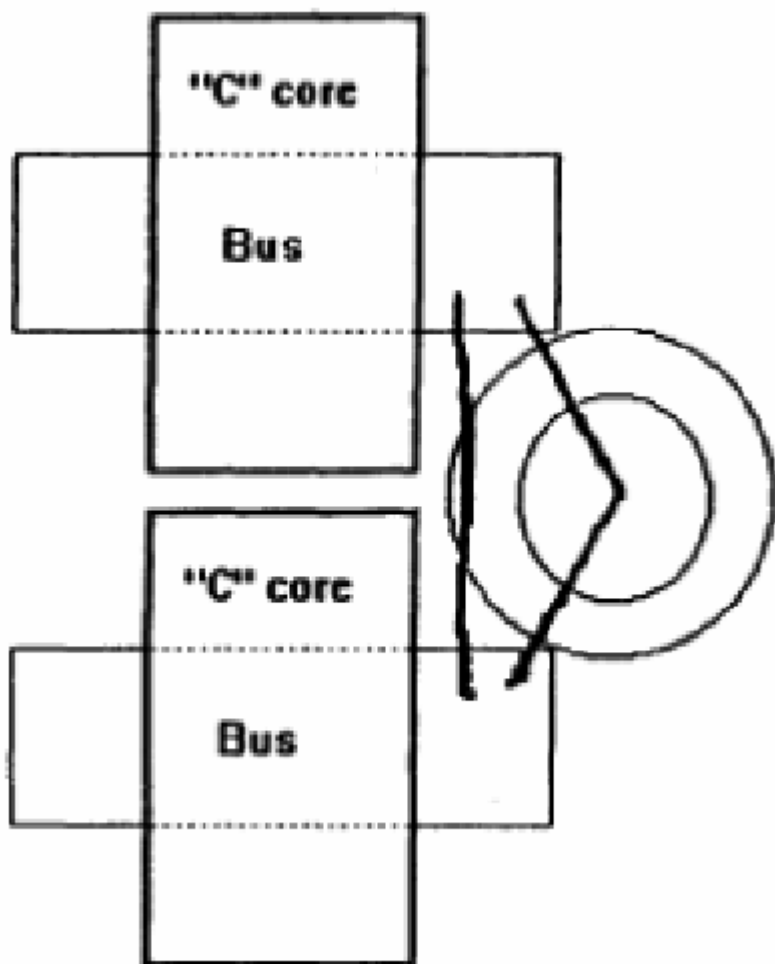


Figure 16.27 High-current filter, alternative method 2.

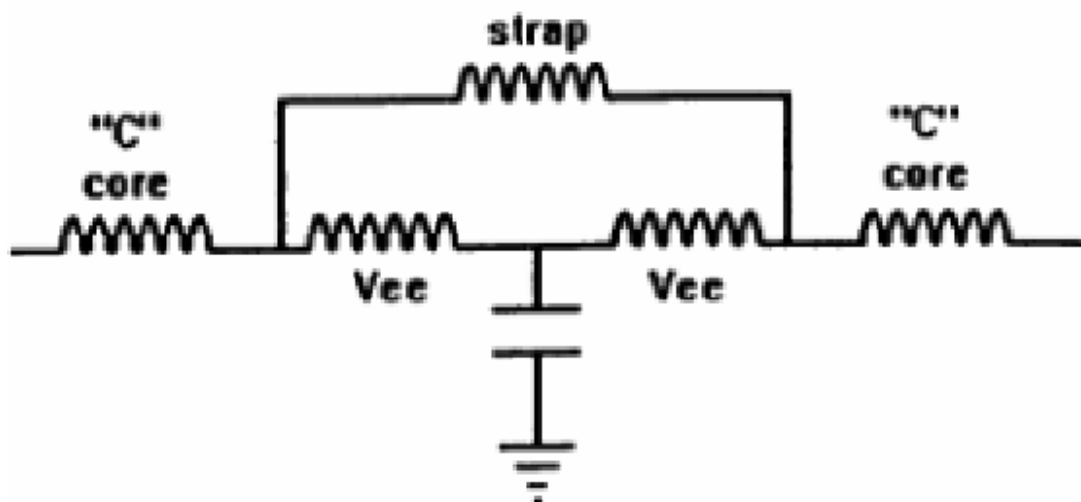


Figure 16.28 The vee capacitor in parallel with shunt wire.

The main thought is to avoid these high-current filters if at all possible. If the designer cannot, parallel the filters so that conventional lower current filters can be used, avoiding high-current design. The objective of this section is to give the designer some thoughts on the design that will help if this situation cannot be avoided. The equations listed earlier are marginal but should get the designer close so that, with minor modifications, the filter will be complete.

当然主要设计思想还是尽可能避免使用大电流滤波器。如果设计者不能做的这一点，就使用并联滤波器的方法，这样就可以使用常规低电流的滤波器了。本节的目的是在设计上给设计者一些思路，以帮助设计者在遇到无法避免使用大电流滤波器时进行设计。前面列出的等式是考虑了余量的，但还是要求设计者能尽量接近这些等式的计算值，这样的设计实际上只需要较小的修改就可以完成滤波器设计。

Another alternative is to replace the feedthrough capacitor with pressed or flattened Y capacitors mounted on a bus connected between the two buses running through the C core (Figure 16.29). The width of the capacitors should be about the same width as the bus, and the buses carry all the current except the leakage current through the capacitors. Several capacitors can be mounted on the bus, giving each capacitor a higher self-resonant frequency. Other advantages are that the overall volume is smaller, the total capacitance is the sum of those along the bus, and Y capacitors do not require torquing after the filter is heat cured even though the output feedthrough requires torquing after filter curing for the best capacitor results. If the capacitors along the bus can be spaced somewhat wider, allowing ample room to solder the leads, capacitors may be placed on both sides on the bus. The upper capacitor bus hole would be between two capacitors on the bottom, for example. The D_x of the capacitor would be narrower, allowing the bus also to be narrower. The cross section of the bus must be the same to carry the full current. The bus can be cut out of thick copper sheet or bolted together. This way, the bus between the C cores may be a different size than the bus through the C cores. Various alternative

methods may be developed using many of these ideas in combination, depending on the situation.

另一个可以选择的方法是，在穿过 C 型磁芯的总线间使用连接总线，并使用可以压接或平面安装到此连接总线的 Y 电容来替代穿心电容（图 16.29）。这个电容的宽度应约等于总线的宽度，且总线承载除通过电容的漏电流以外的所有电流。在这个连接总线上可以安装几个电容，这样这些电容就具有较高的 SRF 值。另外，此方法的另一个优点是总体积可以减小。此滤波器的总电容值就是此连接总线上电容值的和，而且尽管穿心电容需要热愈后调整扭矩以提高电容效能，但是此设计方法的 Y 电容在滤波器热愈（**出厂前需加热滤波器，再调整滤波器以确保实际使用时不用重新调整**—译者注）后并不需要扭矩的调整。如果沿连接总线的电容可以间隔宽一些以便于留出充裕的焊接引线的空间，那么或许可以将电容器置于总线的两侧。例如，上面的电容器总线上的孔可以在下面的两个电容器的中间。电容器的 D_x 应窄些，这样连接总线也可以窄一些。连接总线的截面应与承载满负荷电流的截面相同。或许连接总线由于挖孔的原因会与穿过 C 型磁芯的总线有差异，此时可以依据情况不同选择并结合使用多种设计方法来解决此问题。

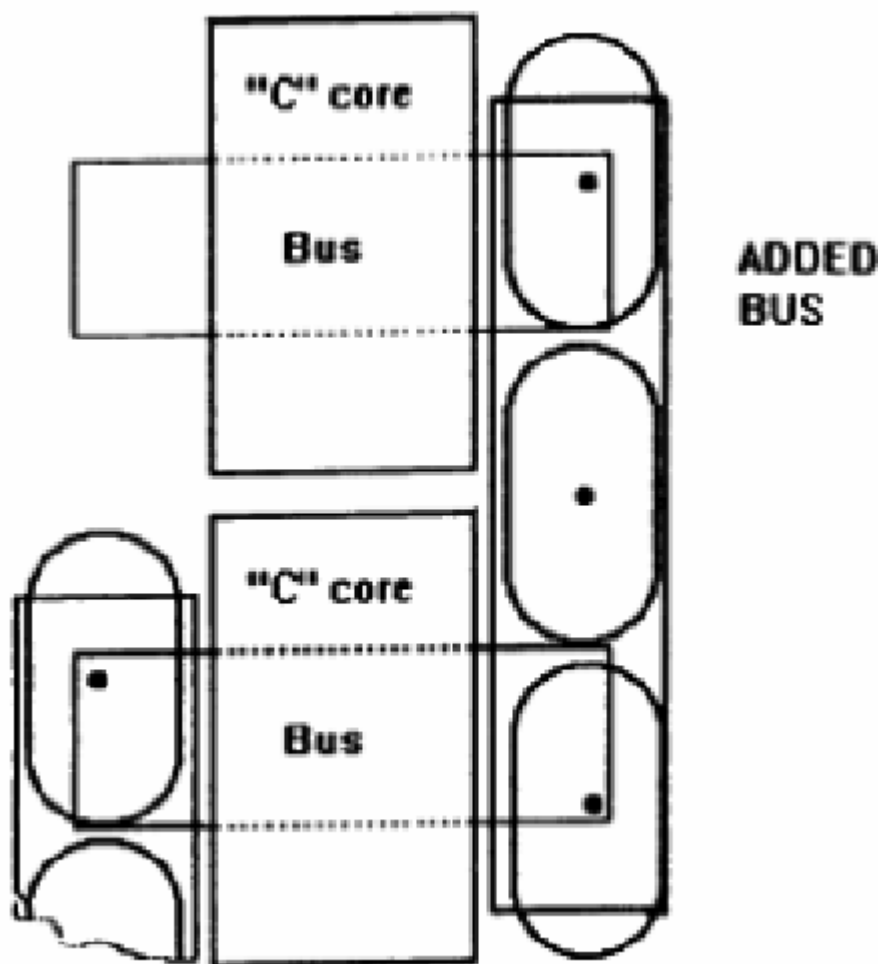


Figure 16.29 The last alternative high-current filter.

Using this suggestion, the inductance along the bus adds to the overall inductance and is similar to veeing. The capacitor lead length is low, making ESL and ESR very low and maintaining the high SRF. The disadvantage is that all the

capacitors are lost during repair or while adjusting for insertion loss if components must be added.

使用此建议的方法，总线的电感就可以加到总电感值中，这与 Vee 电容设计的情况类似。电容的引线长度很短，这就使得电容的 ESL 和 ESR 值很低并保持较高的 SRF。此方法的缺点是，在滤波器修改或为达到插入损耗性能进行电路调整时，如果需要加入新的元件那么所有的电容都不能再次使用了。

EMCARE

17

Packaging Information

封装知识

Packaging is a very important subject and is as critical in the world of electromagnetic interference (EMI) filters as it is in the rest of the electronics arena. Component layout is important in all electronics. Components that are susceptible to H fields must be moved away from these fields, yet the wiring or printed circuit board traces, must be short as possible.

如同在其它电子领域一样，封装在 EMI 滤波器领域中是一项重要和具有决定性的因素。当然在所有的电子产品中元件的布局都是很重要的。电子元件对 H 场很敏感，所以要使元件远离磁场干扰，因此这就需要导线或印刷电路板走线尽可能短。

§17.1 Layout

§17.1 布局

For best performance, the physical layout of the EMI filter should be long and thin. From Fig. 17.1, it is easy to see that the length is greater than the sum of the height and width. In the high current filter shown in Figure 17.1, the toroids are spaced by the value of the capacitor. This removes the tendency toward cross talk or mutual inductance by increasing the distance between the inductive components. Also, note the distance between the dirty and clean end and the clean and dirty end. In Figure 17.2, the output terminals are on the far end, away from the input connector end.

为达到最佳性能，EMI 滤波器的物理结构需要长而薄。通过图 17.1 可以很容易看到，EMI 滤波器的长度远大于高度和宽度的和。在图 17.1 表示的大电流滤波器中，磁环被电容所间隔，这样通过增加感性元件间的间距可以很好地避免磁环间串扰和互感的倾向。另外，需要注意“干净”和“脏”的终端之间的距离。在图 17.2 中，输出端在远端，并且与输入端远离。

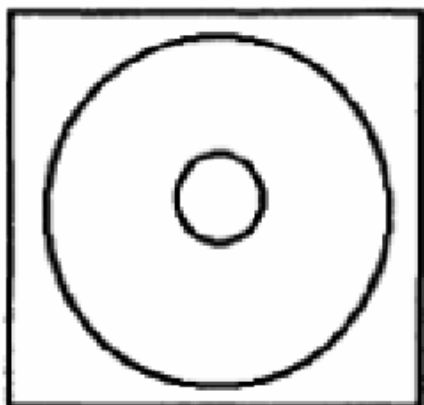


Figure 17.1 High current insert showing the front cover.

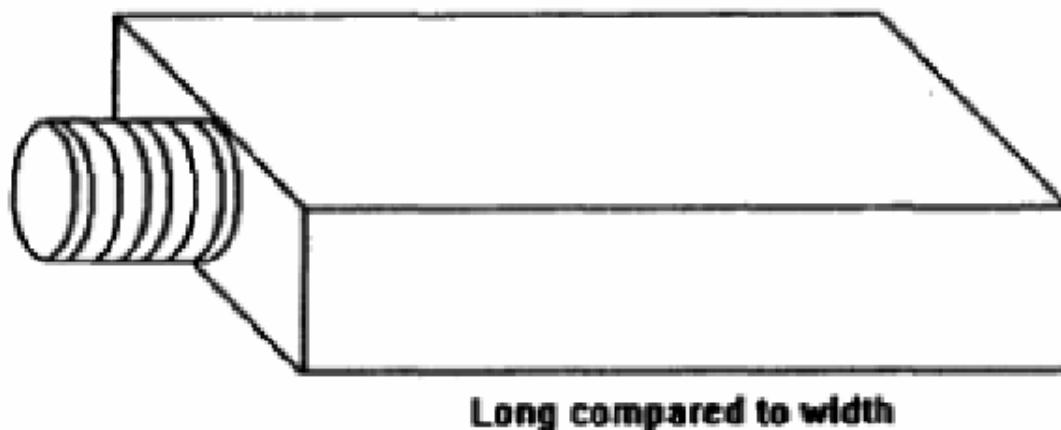


Figure 17.2 Filter showing good length to width ratio.

If the input and output must be on the same face, a shield should run almost the full length of the filter, as shown in Figure 17.3. Half of the components are divided between the two halves. Half run from the front to the back half and then double back to the front on the other side of the shield. The shield must be fully grounded the entire length.

如果输出和输出必须在同一个平面上，那么就需要如图 17.3 的一个屏蔽隔层，这个隔层应几乎与滤波器整体长度一致。在被分割成两半的空间中元件也被分成两部分，一半的元件从前向后排列，另一半元件在屏蔽面的另一侧再折返排列回前面。这个屏蔽面在整个滤波器长度范围内必须可靠接地。

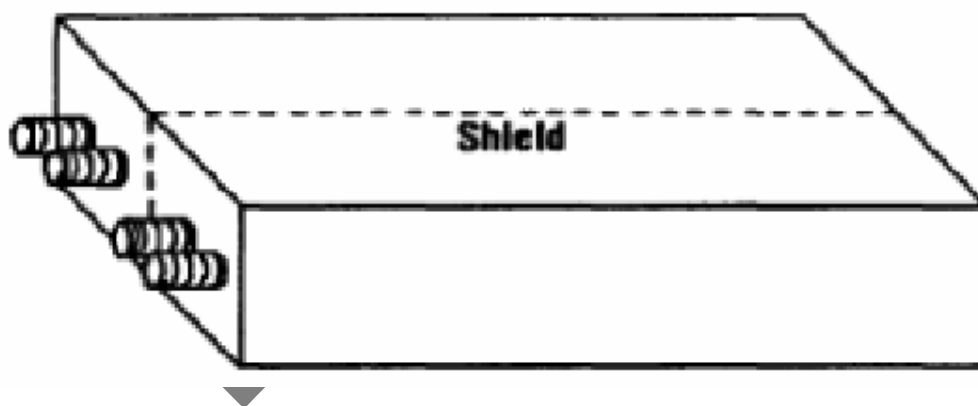


Figure 17.3 Filter showing shield to separate clean and dirty areas.

In the lower current mode, these parameters still hold true. The filter's aspect ratio should be long in length compared with height and width. The components should run from one end to the other, as in a transmission line, rather than zigzagging back and forth within the filter body. This reduces the cross-talk effect. Capcon should be used to cover lead wires to help attenuate the upper frequencies. The inductors should be mounted in quadrature (even toroids), as shown in Figure 17.4 and in the alternative Figure 17.5. The alternative (Figure 17.5) requires more room, but all the toroids are in quadrature; the two toroids

in Figure 17.4 are not, but they are separated by an additional distance. The upper left and the lower right are in the same plane, with a capacitor between them, but the distance is greater, which reduces the magnetic coupling.

在低电流类型的滤波器中，同样需要按这样的参数设计。滤波器还应是长度大于高度和宽度。而且元件的排列就如在同一条传输线中一样，应从一个终端排列到另一个终端，而不是在滤波器内沿 Z 形折返排列，这样就会降低串扰。Capcon 电容的应用应考虑引线，以便于在上限频率条件下满足损耗要求。电感的安装应采用正交的位置（甚至是磁环），具体方法应采用如图 17.4（左右两种方法）和图 17.5 所示（左右两种方法）的方法之一。虽然图 17.5 表示的两种方法需要更多的空间，但能保证所有的磁环都正交排列；而图 17.4 的却不是，但是采用这样的方法却可以增加磁环的间隔距离。如图 17.4 左上和右下的磁环处在同一个平面并有一个电容安装在磁环中间，但是因为磁环间距离很大，这样也就减小了磁场耦合。

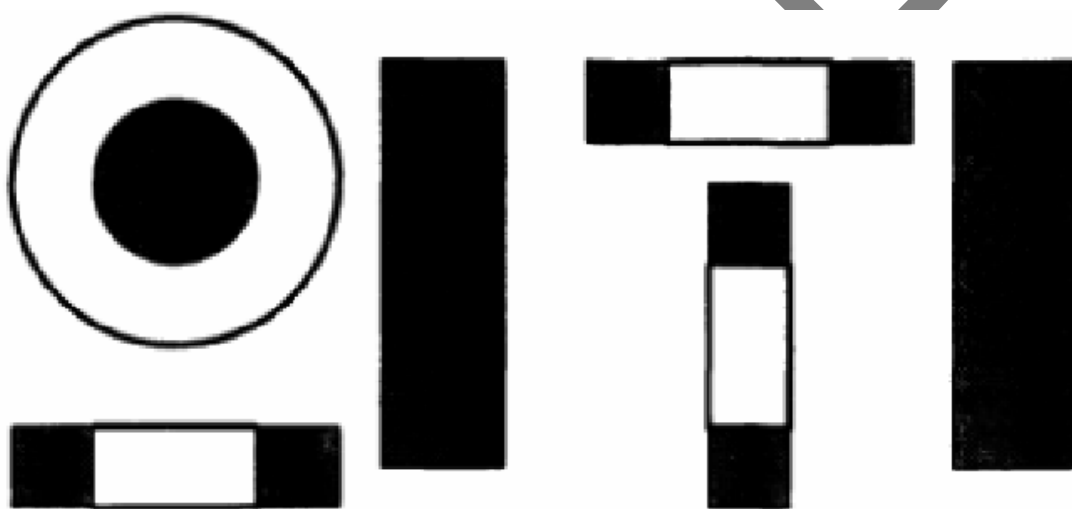


Figure 17.4 Toroids in quadrature.

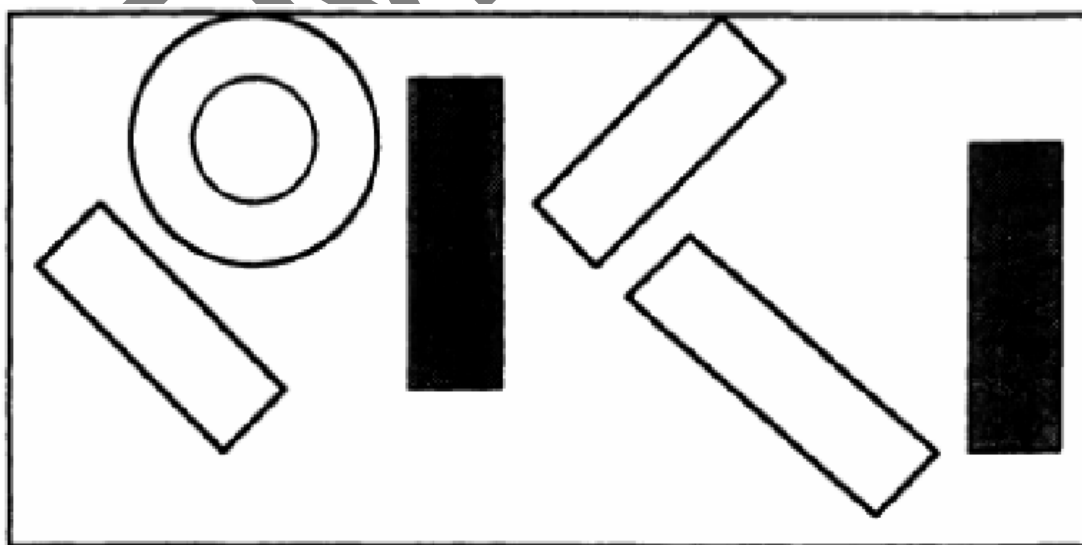


Figure 17.5 Alternative balanced double L in quadrature.

The top two inductors would be wired directly to the line-to-line capacitor and the bottom two also wired directly to the capacitor using the vee technique. See Section 6.1. This continues to the next section, maintaining the quadrature of the inductors. These are not usually mounted to a printed circuit board because of the current and the dc resistance of the boards. Most EMI houses do not design their filters to utilize printed circuit boards.

上面的两个电感可以直接与线间电容连接，而下面的两个可以与 V 型电容（见 6.1 节）直接连接。同样，下一节电路也保持正交的排列方式。注意，这些元件通常不安装在 PCB 上，这是因为使用 PCB 板有电流和 DC 阻抗等因素的限制。因此通常 EMI 设计室并不使用 PCB 设计滤波器。

Some engineers have designed the EMI filter as part of the power input, and this is appropriate if the filter is mounted in a container that is a good conductor and is grounded to the third green wire so that the feedthrough capacitors can function properly. This works well if the needed loss is for Federal Communications Commission standards or the required loss is low. Other designer have placed the filter within the power supply using open, or exposed, components. This technique rarely works. The filter must have shielded components to function properly or other magnetic fields are either influenced by the filter or couple their magnetic field to the inductors of the filter. This way, a 60 dB filter is reduced to only 24 dB and the filter designer does not know what went wrong.

一些工程师将 EMI 滤波器设计成电源输出的一部分，如果滤波器装在一个良导体的壳内，而且通过地线接地（黄绿线），这样穿心电容可以良好工作。当然如果设计满足 FCC 标准的插损要求或是插损要求低的滤波器，这样的设计是适合的。另外还有一些工程师常将滤波器设计在电源上而且滤波器元件是暴露的，那么用此方法设计的滤波器就基本不起作用了。此滤波器必须使用屏蔽了的元件才能使滤波器有效工作，否则其它的磁场就会被滤波器干扰或耦合到滤波器的电感上。这种设计方法会使得 60dB 的滤波器减小到只有 24dB，而且滤波器设计者并不知道错在哪里。

The case or container of the filter must be a good conductor. The better this surface conducts, the lower the magnetic field is on the outside of the case. Even though cold-rolled steel is often used for the filter body, the container is often silver plated to enhance conduction. This attenuates the H field and improves the radiated emissions. The H field establishes a current on the surface of the filter body container. The better this surface conducts and the thicker the case material, the weaker the current on the other side of the case. This reduces the H field departing from the case wall and is true of H fields either from the filter or to the filter. The container must also be a good conductor so that the feedthrough capacitors can function. The same would be true if the good conducting case were not wired to ground or the ground wire were loose or missing. In the circuit in Fig. 17.6, neither the feedthroughs, C_2 , nor the two common mode arresters work properly if the case ground is resistive or the container has a high resistance. The one thing we can say about the ground is

that it isn't ground, or as most say, *ground isn't*. So, grounding of these filters cannot be marginal or overlooked.

滤波器的外壳必须是良导体，外壳表面导电性越好，在壳体外表面上的磁场就越小。尽管常使用冷轧板来制作滤波器壳体，但通常还是要使用镀银的方法来提高导电性。这种处理方法能衰减 H 场并改善传导发射。H 场会在滤波器壳体表面上感应出电流，此时壳体表面导电性越好、壳体越厚，那么在壳体的内表面的电流就越弱。这样就会降低壳体上发射的 H 场，而且对于从滤波器发出或辐射到滤波器的 H 场，都同样有衰减的效果。滤波器外壳需要是良导体，以便于穿心电容正常工作，当然对于壳体没有接地的情况则情况有所不同。在如图 17.6 的电路中，如果壳高阻接地，那么穿心电容和那两个共模避雷器都不能正常工作。这时我们认为此地不是地。所以滤波器接地是不能忽略的。

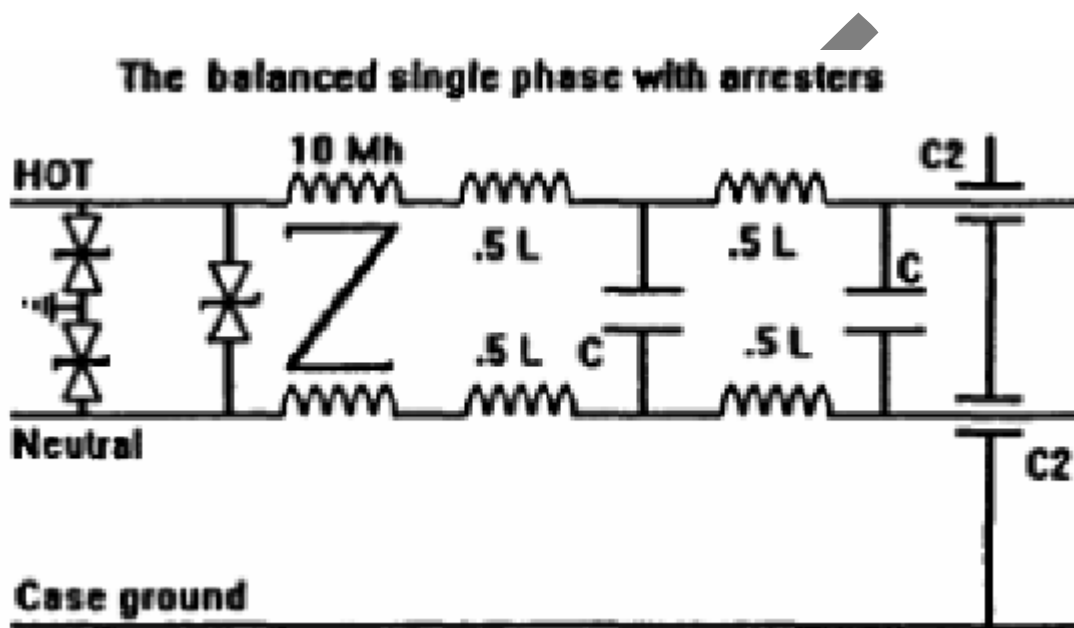


Figure 17.6 Arresters and feedthroughs to ground.

§17.2 Estimated Volume

§17.2 体积的估算

The approximate volume of the higher current filter was discussed in Chapter 16. The equation is repeated here, where S is the number of filter elements (the number of Ls, Ts, or πs). The equation was based on L filters. O_d and I_d are the outside and inside diameters (inches).

在 16 章中我们讨论了大电流滤波器的近似体积。此处重复列出计算的表达式，其中 S 为滤波器元件数（Ls、Ts、πs 的数目）。此等式是基于 L 型滤波器的。 O_d 和 I_d 为内外径（单位：英寸）。

$$L = \frac{0.4U_e(O_d - I_d)WS_f 10^{-8}}{O_d + I_d} = 0.4U_eWS_f 10^{-8}$$

where L is the inductance and S_f is the stacking factor. R, for the capacitor, is
此处 L 为电感， S_f 为占空因数。对于电容，R 为

$$R = \frac{4CKT_t}{p}$$

where C is the capacitance in uF, K is the dielectric constant, and T and t are both thicknesses but T is in mils. This was calculated based on L filters, but T and π filters should be close (these are approximations, anyway).

此处 C 为单位为 uF 的电容, K 为介电常数, T 和 t 都是厚度, 但是 T 的单位为 mil。这同样是按 L 型滤波器的情况而计算的, 但对于 T 和 π 型滤波器则应比较接近 (总之这些都是近似值)。

$$V_{tot} = 1.1S \left[\frac{R}{N(O_d^2 - I_d^2)} + \frac{404.3gNL_{mh}}{O_d S_f} \right] NO_d^2$$

If O_d is much larger than I_d , V_{tot} approaches

如果 O_d 远大于 I_d , 则 V_{tot} 近似为

$$V_{tot} = 1.1S \left(R + \frac{404.3gN^2 O_d L_{mh}}{S_f} \right)$$

On the other hand, McLyman has provided the following data, which are combined in Table 17.1, to calculate many different magnetic properties from his book, *Transformer and Inductor Design Handbook* (Marcel Dekker, New York). Our goal here is volume (volume to weight in the next section). See also Chapter 11. The main idea is to find the area product A_p in centimeters to the fourth power, and from this, and knowing the core, the approximate volume can be found (Figure 17.7). Per McLyman, the energy of the inductor must be determined:

另一方面, McLyman 在他的书 *Transformer and Inductor Design Handbook* (Marcel Dekker, New York) 中提供了一些数据用来计算不同的磁特性, 这些数据列在表 17.1 中。此处我们的目的是计算体积 (体积与重量的比在下一节介绍), 在 11 章中同样也给出了这些内容的介绍。其主要的方法是计算出第四个电源的面积积 A_p (单位: 厘米), 并了解磁芯的参数, 最后就可以计算出近似体积 (图 17.7)。通过 Mclyman 的方法, 电感储存的能量为:

$$ENG = \frac{LI_p^2}{2}$$

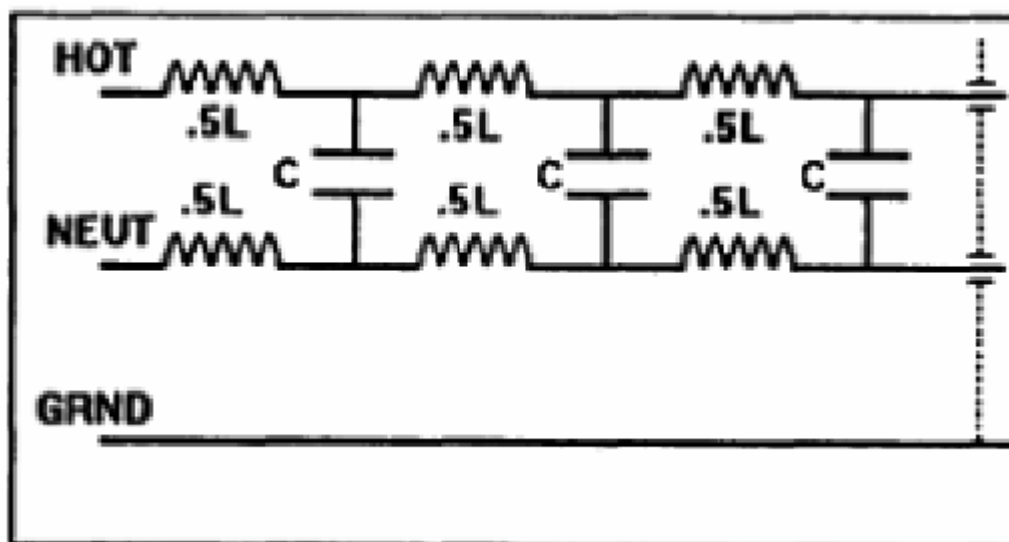


Figure 17.7 Using the McLyman parameters for size and volume.

The type of core to be used must be known to use Table 17.1. K_j and X come from Table 17.1. K_w is the winding factor—0.4 for a toroid and B_m (teslas) must be known for the core type.

使用表 17.1 时必须要知道磁芯的类型。通过表 17.1 可以得到 K_j 和 X 的值。 K_w 是绕线因数——对于磁环为 0.4，对于选定的磁芯类型， B_m （单位：特斯拉）也是已知的。

Table 17.1 McLyman Magnetic Factors Based on Area Product

Core type	K_j 25°C	K_j 50°C	x	$K_j C_m^{-1}$	K_w (g)
Pot core	433	632	1.20	14.5	48.0
Powder core	403	590	1.14	13.1	58.8
Laminations	366	534	1.14	19.7	68.2
C core	323	468	1.16	17.9	66.6
Single coil	395	569	1.16	25.6	76.6
Tape wound	250	365	1.15	25.0	82.3

$$A_p = \frac{[2(ENG)10^4]^p}{B_m K_w K_j}$$

Find the A_p for the different sizes of inductors, and add the different A_p for all the inductors for the total A_p . For example, a three-stage balanced L filter would require six inductors, all of the same value. Find the energy based on the peak current, and from the core type, determine the components for the A_p .

通常对于不同尺寸的电感计算出其 A_p 值，并将所有电感的 A_p 相加得到总 A_p 值。例如，一个三节平衡电路 L 型滤波器需要 6 个电感，6 个电感具有相同的值，并计算出基于峰值电

流的储存能量值，最后通过磁环类型的不同确定出元件的 A_p 值。

If the peak current is 5 amps and the inductors are 250uH,
如果峰值电流为 5 安培并且电感为 250uH, 那么

$$ENG = \frac{250 \times 10^{-6} \times 5^2}{2} = 0.0031$$

If MPP powder cores are the choice, then $K_w=0.4$, K_j at $25^\circ\text{C}=403$, $B_m=0.7\text{T}$, and $X=1.14$.

如果选择 MPP 粉芯环, 那么 $K_w=0.4$, K_j @ $25^\circ\text{C}=403$, $B_m=0.7\text{T}$, $X=1.14$ 。

$$A_p = \frac{(2 \times 0.0031 \times 10^4)^{1.14}}{0.7 \times 0.4 \times 403} = 0.9792$$

Round this to 1, and find the total A_p and then the volume:

将此值近似为 1, 并计算出总的 A_p 值, 那么体积为:

$$V_{L_{\text{tot}}} = 1 \times 13.1 \times 6 = 78.6 \text{ cm}^3$$

where 13.1 is from Table 17.1 for the MPP core in cubic centimeters. The capacitors are not included, but the weight ratio of the capacitors is of the order of that of the inductors. The total is 160 cm^3 , and this volume is only 60% utilized. This gives 267 cm^3 , but allow for the container, feedthroughs, and wiring requires being rounded to 280 cm^3 . This equates to 17 inches^3 . These are rough estimates that should get the design engineer in the ballpark.

此处 13.1 是通过表 17.1 中 MPP 磁芯的数据得到的, 单位是立方厘米。因为实际上电容的重量与电感相比相差一个数量级, 所以计算上没有考虑电容。计算出的总数为 160 cm^3 , 如果体积按只利用 60% 计算, 那么实际需要 267 cm^3 。考虑到壳体、穿心电容和导线的要求, 可以近似为 280 cm^3 , 等于 17 in^3 。当然这是粗略的估算, 只是给设计这一个大致的范围。

§17.3 Volume-Weight Ratio

§17.3 体积—重量比

Bob Hassett at RFI Corp. (Bay Shore, Long Island, NY 11706), has done some research on the size to weight ratio for EMI filters. These were primarily done on the tubular types of filters mentioned in an earlier chapter. The ratio is 1.5 ounces per inch^3 . This equates to 1.6 pounds for the filter just discussed, which needed 17 inch^3 .

RFI 公司的 Bob Hassett (Bay Shore, Long Island, NY 11706) 针对 EMI 滤波器的尺寸重量比进行了一些研究。先前的章节中我们对管状滤波器进行过介绍, 其比值为 1.5 盎司/立方英寸。对于我们刚才讨论的滤波器, 其 17 立方英寸的体积就需要 1.6 磅的重量。

Again, use McLyman's area product and the same A_p as for one inductor. Multiplying this value of 58.8 for each inductor by the six inductors, as listed for the powder cores in grams,

另外, 利用 McLyman 的面积积参数和单个电感的 A_p 值。将每个电感的值 58.8 乘以 6 (电感个数), 得到粉芯的重量 (单位: 克):

$$58.8 \times 6 = 352.8g$$

Doubling this for the capacitors, wiring, feedthroughs, container, and input terminals,

考虑到电容、导线、穿心电容、壳体和输入端子等对重量的影响, 现将此值加倍:

$$352.8 \times 2 = 705.6g$$

The weight in pounds is

转换成磅的单位为

$$\frac{705.6}{459.53} = 1.535 \text{ pounds}$$

This looks like the same ballpark where RFI Corp. plays, even though McLyman is at the NASA Jet Propulsion Laboratory in Southern California and Bob Hassett is in Bay Shore on Long Island, New York. Anyway, their two methods are close to agreement.

这个结果类似于 RFI 公司的计算结果, 对于 McLyman 和 Bob Hassett, 他们的这两种方法是比较吻合的。

18

Questionable Designs

有问题的设计

The designs in this chapter have been around for years: I have no idea of the initial group or company that designed them. The reason that they are here is for your critique, and the hope is that you come to the same view as most filter designers.

本章列出的设计已经是好多年的设计方案了，所以我并不知道最初设计这些方案的是哪些公司。此处列出这些方案是为了通过批评这些方案，使得你能避免犯许多设计者犯下的同样的错误。

§18.1 28V at 35A

§18.1 28V @ 35A 滤波器

The high current in Figure 18.1 suggests low values of inductance and high values of capacitance. C_1 at 88 μ F is way too high and would be, at best, resistive, inductive at any reasonable switcher frequency, and yet this filter has four of them. They add weight, volume, and cost with little electromagnetic interference (EMI) benefit.

图 18.1 中的大电流滤波器采用低电感值和高电容值。但是 88 μ F 的选值太大了，此电容会在任何常见的开关频率下表现为阻抗或感抗，而且此滤波器还有另外 4 个这样的电容，这些电容会增加滤波器的重量、体积和成本，但却几乎起不到 EMI 衰减功能。

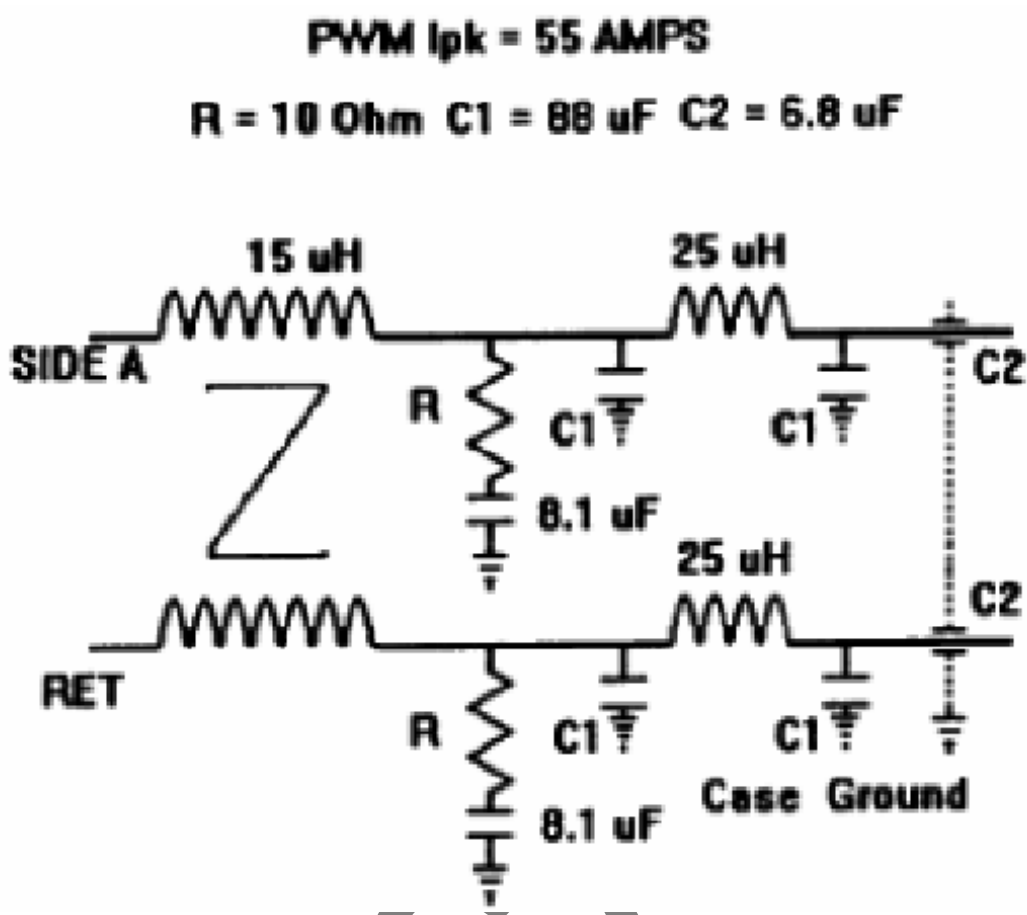


Figure 18.1 DC filter, 28V at 35A.

The RC shunt, composed of the 10Ω resistor and the $8.1\mu\text{F}$ capacitor, kicks in at 2kHz , showing that the switcher frequency—or the current pulse—is well above this frequency, as are most nowadays. The resistor should be nearer the design impedance of 0.8Ω . This drops the capacitor value to $1\mu\text{F}$, again reducing the weight, volume, and cost but also raising the self-resonant frequency (SRF). The 10Ω resistor and the $8.1\mu\text{F}$ capacitor, along with the 0.8Ω and the $1\mu\text{F}$, would give little help to the $6.8\mu\text{F}$ feedthroughs. The 0.8Ω and the $1.0\mu\text{F}$ would offer a higher impedance, but not that much more. The $6.8\mu\text{F}$ almost stands alone.

由 10Ω 电阻和 $8.1\mu\text{F}$ 电容组成的 RC 旁路作用频率在 2kHz 以下，而开关频率（或电流脉冲频率）在当今的应用中远高于此频率。实际上，电阻应接近设计阻抗 0.8Ω ，电容应降为 $1\mu\text{F}$ ，这同样会减小重量、体积和成本，而且会提高 SRF 值。 10Ω 和 $8.1\mu\text{F}$ 电容的 RC 旁路以及 0.8Ω 和 $1\mu\text{F}$ 电容的 RC 旁路都几乎不会对 $6.8\mu\text{F}$ 的穿心电容有辅助作用， 0.8Ω 和 $1.0\mu\text{F}$ 将提供一个较高的阻抗，但没有前者没有那么大。实际上， $6.8\mu\text{F}$ 电容几乎是孤立的。

The inductors add little common mode loss to the filter. In most applications, the Zorro would be at least an order of magnitude above the $15\mu\text{H}$ inductor in the circuit in Figure 18.1, where the two differential inductors contribute $12.5\mu\text{H}$ to the common mode (the same order of magnitude), giving a total $27.5\mu\text{H}$.

This makes for a rare design.

这些电感对滤波器的共模损耗几乎没有作用。在多数应用中，图 18.1 中的 Zorro 电感值至少要比 15uH 大一个量级。此处两个差模电感对共模贡献 12.5uH 的电感（与共模电感量级相同），总电感为 27.5uH。这种取值造成了一个比较少见的错误设计。

There is some differential, with the two balanced inductors totaling 50uH and the two feedthrough in series giving 3.4uF. The impedance is 3.8Ω , and the cutoff is 12.2kHz.

对于差模这个设计方案有一些作用，平衡电感的总电感量为 50uH，两个穿心电容串联为 3.4uF。阻抗为 3.8Ω ，并且截止频率为 12.2kHz。

§18.2 60Hz and 120V with Transorbs

§18.2 120V/60Hz 应用条件下带 transorb 管的滤波器

Figure 18.2 shows another case in which the differential inductor is larger by two orders of magnitude over the common mode inductor. The two differential inductors give 1.2mH of common mode, so the 15uH adds no real support for this situation. The 15uH is smaller than the error of these two differential components. It seems that the two inductors are misnamed. The two 2.4mH should have been the common mode and the two 15uH inductors the differential mode inductors.

图 18.2 给出的是另一个设计案例，在此案例中差模电感比共模电感高两个量级。这两个差模电感等效为 1.2mH 的共模电感，因此 15uH 的电感在此情况下是没有实质作用的。此例的错误是，选取了比个差模电感值小很多的共模电感，看上去像是两类电感标错了位置，而 2.4mH 应该是共模电感，15uH 应是差模电感。

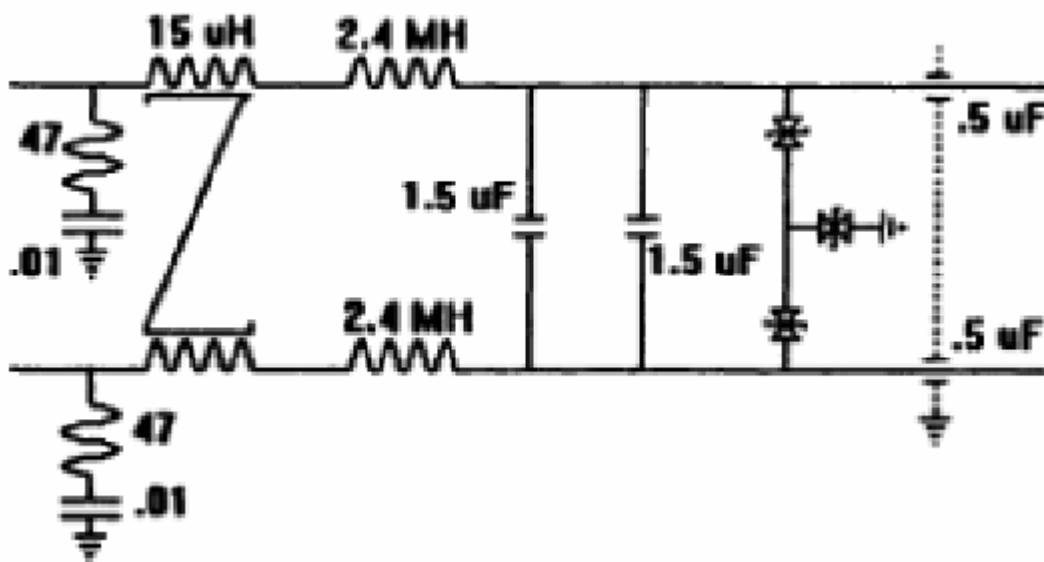


Figure 18.2 60Hz with 120V and transorbs.

The two RC shunts are not correct, either. The 47Ω may be high unless the design impedance is around 47Ω , and the capacitor is too low. The attenuation of this RC shunt starts at 240kHz, so it will not help with any switcher noise or most of the parasitic noise.

disadvantage of using most analysis programs because most treat these as pure capacitors well into the GHz realm. Some programs allow the designer to add this information, but most enter the component information as if they were pure capacitors. Those that would do so are often not aware of the true property of the component.

从 EMI 的观点来, 无论如何这三个大电容是无用的。早在可能有 EMI 需求的频率以前, 它们就已经变为感性的了。这种错误常常是由仿真软件的缺陷造成的, 多数的仿真软件把电容当成能在 GHz 频率范围良好工作的理想电容。虽然一些软件允许设计者增加元件信息, 但是输入的信息多数都误当作理想电容来处理了。因此这种处理忽略了元件的真实特性。

The two RC shunts are almost useless. They do not come into play until 720kHz, which is well above most switcher frequencies and their harmonics and above most parasitics of the switcher transformers and/or inductors. If there is a high-frequency problem with this filter, the 47 Ω resistor does not help. The value should be closer to the load impedance, which should be near the design impedance of the filter. This should be closer to 4.5 Ω .

那两个 RC 旁路几乎没有用处。直到 720kHz 它们才会起作用, 但是这个频率远在多数开关频率及其谐波频率和开关电源的变压器或电感的寄生振荡频率之上。如果有一个高频问题, 那 47 Ω 电阻对解决此问题没有帮助, 实际上其值应与负载阻抗接近, 同样滤波器的设计阻抗也应与负载阻抗接近, 此例中, 电阻应接近 4.5 Ω 。

The 0.1 μ F capacitors to ground should be feedthroughs for better SRF and should be located on the load side. These two capacitors in series across the line give a line-to-line value of 0.05 μ F. This adds to the input capacitor of the balanced π for a total of 0.15 μ F. If the leakage inductance of the Zorro is small and if the line impedance is small, this renders the 0.15 μ F useless well into the upper kHz range. This is not a VDE, Federal Communications Commission (FCC), or CSA filter because the component count is too high for these types. If losses are required in the lower kHz range, this technique is not valid. If this filter were tested using the 220A specification or some of the better LISNs, creating a line impedance in the lower kHz range, this filter would look good. This is, again, why the π filter should be limited in use.

另外, 0.1 μ F 的对地电容应是具有较好 SRF 的穿心型, 并且应置于负载侧。这两个对地电容串联后并接于线间等效为 0.05 μ F 的线间电容, 这会令平衡 π 型滤波器的输入电容增加到 0.15 μ F。如果 Zorro 的漏感很小且线路阻抗也很小, 那么会导致 0.15 μ F 电容在 kHz 范围里失效。这个滤波器不是面向 VDE、FCC 或 CSA 标准的滤波器, 因为对于这些标准此滤波器的元件数太高了。如果使用 220A 规范来测试或使用一些能在 kHz 范围内有一定线路阻抗的 LISN, 那么此滤波器性能良好。这也是 π 型滤波器应被限制使用的另一个原因。

If the 0.5 and 120 μ F are designed to lower the dc supply impedance, this network should be moved to the load side: why lower the impedance and then raise it by the two 12.5 μ H inductor? However, the 120 μ F is too large to reduce the switcher droop, and so is the 2400 μ F. The best solution would be to remove

these four components along with the two RC shunts. Move the capacitors to ground, as stated earlier, and then double the size of the output π capacitor. This makes this an L filter, all that is possible, anyway, at a 1.414 times higher cutoff frequency. The circuit now looks like Figure 18.4.

如果使用 0.5 和 120 μ F 电容来降低 DC 电源阻抗,那么这些电容应使用在负载侧,那么这个解决方案就很矛盾,为什么降低阻抗后又用两个 12.5 μ H 的电感来提升阻抗呢?而且 120 μ F 的电容太大了,以至于开关电源的输出受到严重衰减,同样对于 2400 μ F 的电容也存在这个问题。最好的解决办法是将这 4 个元件和两个 RC 旁路去掉,按前面的论述应对地电容移到负载端,并且把原图 (18.3) 滤波器的输出端电容增大一倍。这样就形成了一个 L 型滤波器,只有在截止频率的 1.414 倍的频率以上,都会起到很好的效果。此时电路就会如图 18.4 表示的那样。

With all the space saved, the 0.1 μ F could become a 6.8 feedthrough, aiding the 0.4mH Zorro and raising the 12.5 to 56 μ H to make this a balanced T. Careful here, though: this could add to the switcher droop. Add another 0.2 μ F, and make this a double balanced L. More must be known to design this properly, such as the switcher frequency, the on time of the pulse, and the current peak during this time. In other words, this circuit changes and the circuit in Figure 18.4 will not function, but neither will the circuit in Figure 18.3, which must be fully redesigned.

为了节省空间可以将 0.1 μ F 的电容换成 6.8 的穿心电容,将 12.5 μ H 电感增加到 56 μ H,使得电路变成平衡 T 型。此处要注意:这会使开关电源的输出出现衰弱现象。增加另一个 0.2 μ F 的电容,使电路变为双 L 型。如果想得到恰当的设计方案,那么还需要了解更多信息,如开关频率、脉冲持续时间、电流峰值等。换句话讲,如果开关电源电路改变了,图 18.4 的电路就有可能不能正常工作,当然此时使用图 18.3 的电路同样也不行。可以说图 18.3 的电路需要彻底地进行重新设计。

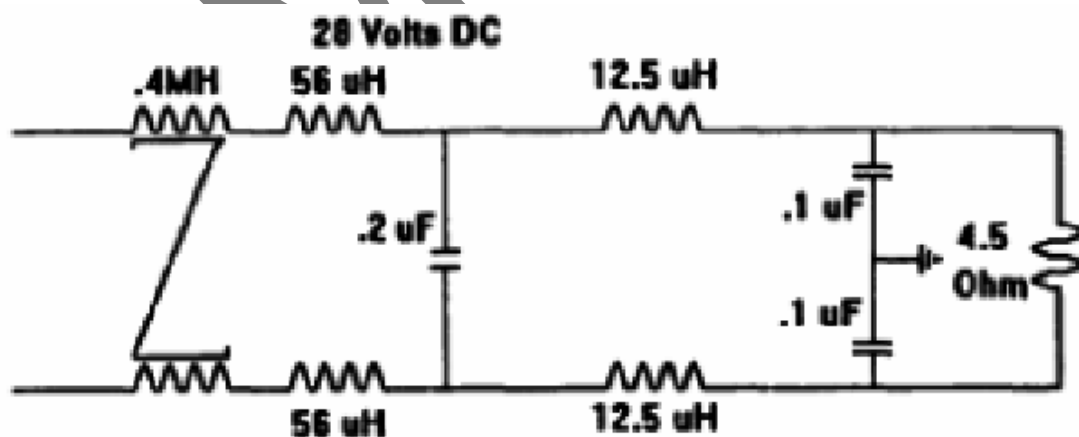


Figure 18.4 The modified 28V dc filter.

§18.4 120V AC 400Hz

§18.4 120V / 400Hz 使用条件下的交流滤波器

The main complaint is that there is no real common mode or differential mode in the filter shown in Figure 18.5. The RC shunt's minimum impedance is 453 Ω ,

giving little aid to the common mode or differential. The same is true of the 4700pF to ground. This may have been a medical application requiring low capacitance to ground for low patient current. The current of nearly 1A agrees with this. This filter gives 6dB per octave for both common and differential modes. If the 800uH (the bottom and top 400uH to convert to unbalanced) is correct, a 0.05uF tied line to line after the inductors would give over 40dB loss at 450kHz for the FCC.

此方案的主要问题是，在如图 18.5 的滤波器中并没有真正的共模和差模电路。RC 旁路的最小阻抗为 453Ω ，这对共模和差模损耗性能几乎没有作用。同样对地的 4700pF 电容也存在问题，因为此滤波器如果用在医疗设备上就会有漏电流过高的问题。对于共模和差模此滤波器的损耗均为 6dB/倍频。如果 800uH（顶部和底部的 400uH 转换为非平衡电路的电感量）的电感量是恰当的，那么对于 FCC 标准的要求，在此电感后接一个 0.05uF 的线间电容，就会在 450kHz 达到大于 40dB 的插损。

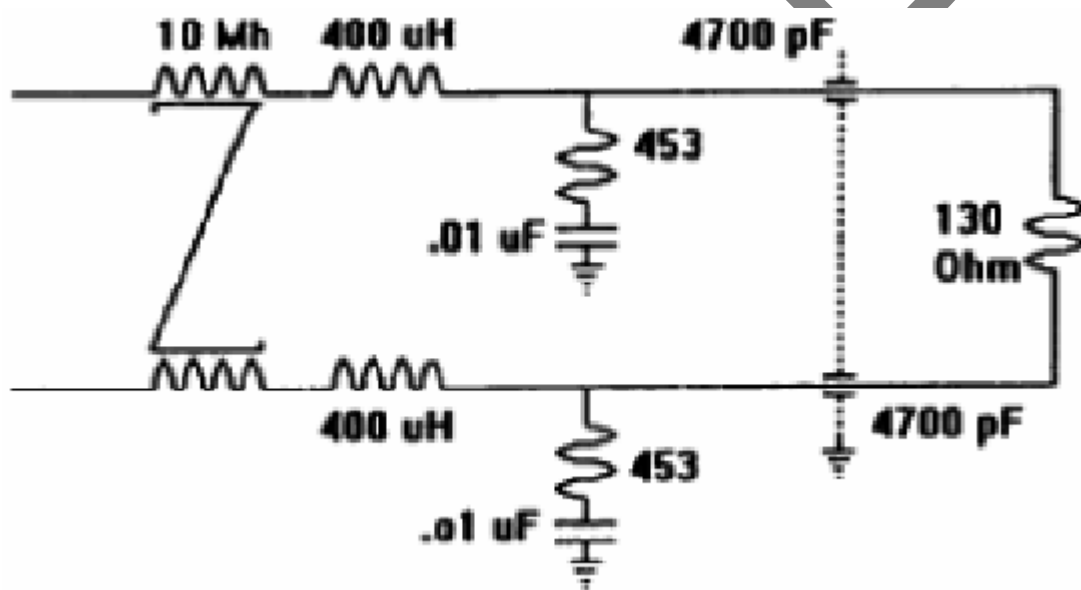


Figure 18.5 The 120V 400Hz filter.

If this is not for medical uses, change the 4700pF for the limit of 0.02uF, the legal limit for 400Hz. This is an order of magnitude larger. Now, with the added 0.05uF from line to line, there are both common mode and differential mode losses. If the two RC shunts are present for a problem frequency, the 453Ω resistor is too high. Change these two resistors to 130Ω each. One of these RC networks, wired from line to line, may replace both networks to ground. Otherwise, omit the RC shunts. The changes are shown in Figure 18.6. Now, the filter has 10mH and 0.04uF making up the common mode half and 800uH and 0.05uF making up the differential mode half. The common mode design impedance is 500Ω and the cutoff is 8kHz; the differential mode impedance is 130Ω , with a cutoff frequency of 25kHz.

如果此滤波器不是用在医疗设备上，那么按 400Hz 的标准限制应将 4700pF 换成 0.02uF 的限制值。这会比原来的电容大出一个量级。现在，在线间增加了 0.05uF 的线间电容后，电路就同时具有了共模和差模的损耗。如果这两个 RC 旁路是为消除一个问题频点设计的，

那么 $453\ \Omega$ 的电阻就太大了，需要将这两个电阻换成每个 $130\ \Omega$ 的电阻。可以用一个这样的 RC 旁路接在线间替代两个 RC 旁路对地的接法。否则就干脆忽略 RC 旁路。变化后的电路如图 18.6。现在，此滤波器由 10mH 和 $0.04\mu\text{F}$ (Y 电容并联等效电容—译者注) 电容组成共模电路而 $800\mu\text{H}$ (两个差模电感串联等效电感—译者注) 和 $0.05\mu\text{F}$ 电容组成差模电路。共模电路的设计阻抗为 $500\ \Omega$ 且截止频率为 8kHz ；差模电路的设计阻抗为 $130\ \Omega$ 且截止频率为 25kHz 。

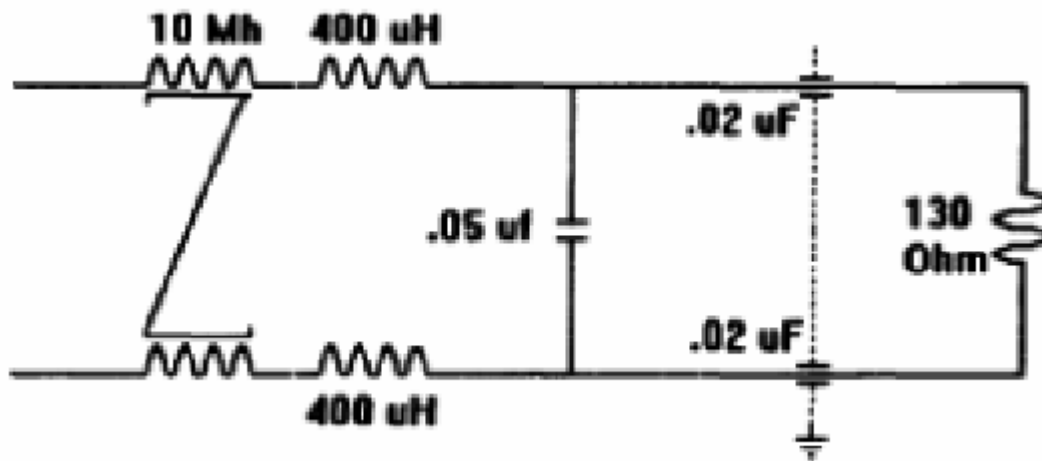


Figure 18.6 The modified 115V 400Hz filter.

§ 18.5 Review

§ 18.5 回顾

It is impossible to look at a filter after the fact and judge it fairly. We do not know all the parameters of the filter. For medical, 461, and 220A specifications only, resonance rises at some unknown frequencies, with information provided to the designer either initially or during some EMI test.

因为我们并不了解滤波器的所有参数，所以在考虑实际使用条件后检查滤波器并判断设计是否合理是十分重要的。对于医疗、461 和 220A 规范，早期的和 EMI 测试中提供的信息会发现一些未知频率点下的增益。

19

Review of Filter Design

滤波器设计回顾

This last chapter discusses some ideas that were mentioned earlier but were not clarified. First, the full design technique is reviewed.

在最后一章我们会讨论一些前面提到过但没有明确的思路。首先，先回顾一下整个设计方法。

§19.1 Filter Design Review

§19.1 滤波器设计的回顾

This is an overview of all the design information in this book with references to the chapter that discusses the subject.

这部分是参考各章主题对本书所有设计的一次汇总。

Before designing the filter, the following should be known: The power line frequency if ac, minimal RMS line voltage, maximum RMS load current, type of load, and lowest switcher frequency if more than one. Some of this can be guessed. If this is a single-phase 60Hz line, a minimum of 100V RMS should do and the RMS line current could be raised by 10%. Attempt to determine the type of load this filter must feed, though: off-line regulator, power factor correction circuit, inductive input filter, or resistive. For a dc system, the load should be a switcher. If this filter is being designed for multiple use or for filter sales, the worst cases from previous chapters should be accounted for within the design. 在设计滤波器之前，需要了解以下内容：如果是交流应用，则要了解电源线频率、最低 RMS 线电压、最大 RMS 负载电流、负载类型和最低开关频率（如果有多个开关频率的话）。一些参数是可以预计的。如果这是一个单相 60Hz 的电源，应是 110V 的 RMS 电压且 RMS 线电流需要增加 10%（这是国外电源情况，国内则应为 220V/50Hz—译者注）。另外需要试着判断滤波器所接负载的类型：离线调节器、电源功率校正因数电路、感性或阻性输入滤波电路。对于一个交流系统，则负载多为开关电源。另外，如果此滤波器为考虑销售而进行了多用途设计，那么就需要在设计中考虑前面章节讨论的最差情况。

1. Find the best filter type from Section 12.3 by knowing the type or needs of the load. Also, the specification will help here. Knowledge of the specification and losses required will help in assigning a line impedance (also Section 12.3); The Federal Communications Commission specifies a higher line impedance because the loss requirements are at frequencies that will give a higher line impedance.

1、在了解负载的类型后，通过 12.3 节的方法可以找到最佳的滤波器类型。同样，规范的

要求也会对设计有所帮助，插损规范的要求会帮助我们确定电源线阻抗（参考 12.3 节）；FCC 规定了较高的电源线阻抗，因为在规范损耗要求的频率下，电源线会是高阻抗状态。

2. Calculate the design impedance from the lowest voltage divided by the highest current.

2、通过用最低电压除以最高电流来计算设计阻抗。

3. Determine the filter cutoff frequency, both differential and common mode. Use either the matrix equations in Chapter 13 or 14 or Section 15.4 on F_0 the easy way. The second method will get the filter designer on the proper ballpark property and the first will get the designer onto the playing field. This can be a computer program written by the reader based on Chapters 13 and 14. (It also can be purchased through the author at a savings as a result of the purchase of this book.) For the first method, the actual equations for the cutoff frequency are

3、确定滤波器的共模和差模的截止频率。可以使用 13 章或 14 章的方法，或使用 15.4 节对 F_0 的简便计算方法。第二种设计方法会使设计者如同置于棒球场的情况，而第一种设计方法则如同置设计者于运动场。对于第一种设计方法，可以由读者自己按 13 章和 14 章的内容编写成计算机程序（同样也可以通过购买本书的随书光盘获得作者书写的程序）。对于第一种方法，截止频率的计算表达式为

$$L = \text{Loss for } p \text{ or } T = (2N+1)6$$

$$L = \text{Loss for an } L = 12N$$

The first equation is for the T or π filter and the second equation is for the L. Either of these equations provides the value of L for the equations that follow. N is the number of filters in tandem.

第一个等式是针对 T 型或 π 型的，第二个等式是针对 L 型滤波器的。这两个等式都会计算出下面等式中的具体的 L 值。N 为滤波器层叠数目。

Loss required	= dB		
Loss per octave for filter	= L		
No. of octaves	= X	= dB/L	
Frequency at needed loss	= F		
Cutoff frequency	= F_0	= $F/2^x$	= $F/2\tau$

Another way to select the value for the loss L is as follows. Choose the loss based on the filter type. Table 19.1 lists the loss per octave for the filter type listed on the left, the value of loss L in the preceding equations.

另一个选择损耗 L 值的方法是，可以基于滤波器类型来选择。表 19.1 列出了相关滤波器类型的每倍频的损耗。

Table 19.1 F the Easy Way: Loss per Octave Based on Filter Type and Units in

Tandem

Filter	Number of filters in tandem						
	1	2	3	4	5	6	7
L	12	24	36	48	60	72	84
π	18	30	42	54	66	78	90
T	18	30	42	54	66	78	90

Once 10 times the power line frequency, or more, is reached, the filter type and the cutoff frequency are known. For example, for three frequencies provided by an electromagnetic interference test house, the approximate dB losses required to meet the specification and the associated peak frequencies are listed in Table 19.2. If the power line frequency is 60Hz, the single L filter will work and the cutoff frequency is 1.4kHz, but if the power line frequency is 400Hz, the single L must be replaced by the double L filter at 12.98kHz. Round either of these to a convenient lower frequency. The filter cutoff frequency is often determined by the lowest problem frequency. Be careful, because exceptions occur, as in the preceding example, so all listed problem frequencies must be checked. Do not assume that it is only the lowest frequency listed that will give the proper cutoff frequency.

一旦每次折半的频率最后延伸到 10 倍于电源线频率以上, 那么滤波器的类型和截止频率就确定下来了。例如, 对于 EMI 测试室提供的三个频率点, 满足规范要求的近似 dB 损耗和相关的峰值频率点列在了表 19.2 中。如果电源线频率为 60Hz, 那么单 L 型滤波器就能满足要求且其截止频率为 1.4kHz, 但是如果电源线频率为 400Hz, 那么就需要在 12.98kHz 下使用双 L 型滤波器来代替单 L 型。将这两个频率各自近似为常规的较低频率。另外, 通常滤波器的截止频率一般由最低的问题频率点确定。注意, 考虑到如前述的例外情况, 所有以有列出的问题频率都应进行检查, 而不应假想只靠列出的最低频率就能确定合适的截止频率。

Table 19.2 F_0 to Evaluate the Required Filter (Single L and Double L)

Test house trouble frequencies	F_1	F_2	F_3
Frequencies	36 kHz	80 kHz	120 kHz
Measured needed loss	30 dB	52 dB	71 dB
Add 6 dB for head room	36 dB	58 dB	77 dB
F_0 for 60 Hz - okay single L	4.5 kHz	2.8 kHz	1.4 kHz
F_0 - double L required for 400 Hz	17.2 kHz	14.98 kHz	12.98 kHz

4. Equate the component values from steps 2 and 3 using the following equations. R_d is the design impedance. This is the proper equation for all filters, π , T, and L. The difference is that the value of the inductor is divided, or split,

for the T, and the value of C is divided or split for the π :

4、在第 2 和第 3 步后用下列等式来计算元件值。其中 R_d 是设计阻抗。这个等式对所有类型的滤波器 (π 、T 和 L) 都适用。不同之处在于对于 T 型滤波器，电感的值是拆分的，且对于 π 型滤波器 C 的值也是拆分的：

$$L = \frac{R_d}{2pF_0} \quad C = \frac{1}{2pF_0 R_d}$$

In a multiple T filter, the first and last inductors are half this value, but the values of the central inductors are the full value. Remember also that the value of the capacitor above, is also divided for the π . Again, the central values for the capacitors for a multiple π will be the whole value and the first and last capacitors will be split. The T and the π filter are exactly opposite each other. Choose the filter layout based on Chapter 6 and on some information also in Chapter 3. Balance the filter if possible.

在多级 T 型滤波器中，第一个和最后一个电感值是此式计算值的一半，但是中间电感的值等于此计算值。对于 π 型的电容与多级 T 型的电感处理方法相同，同样最前和最后的电容是计算值的一半，而中间的电容等于此计算值。由此可以看出，T 型和 π 型滤波器的计算方法是相反的。基于第 6 章和第 3 章的一些内容可以确定滤波器的布局。如果可能的话，应尽量采用平衡电路的滤波器设计。

5. Find the size of the components. Use McLyman's data in Chapters 16 and 17, or design the components (see Figure 19.1).

5、确定元件的尺寸。可以使用 16 章和 17 章由 McLyman 提供的数据或直接设计元件的尺寸 (见图 19.1)。

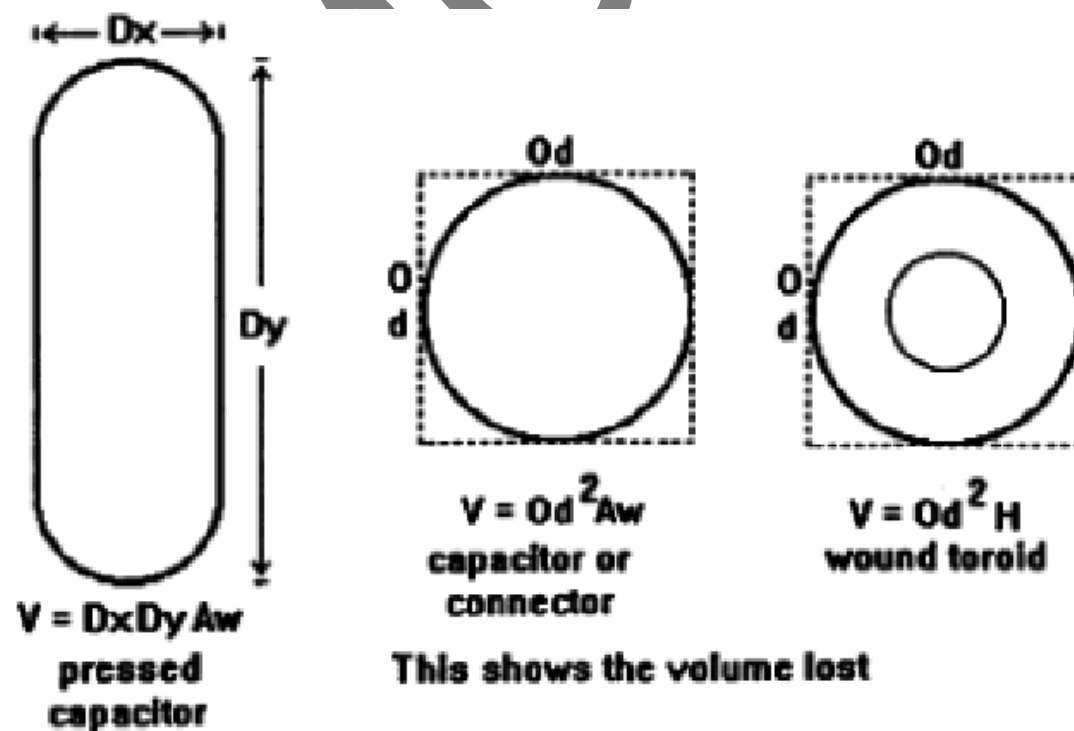


Figure 19.1 Volume of components to calculate total filter volume.

For connectors, round capacitors, or any round components, the Q_l is the square times the length. For a pressed capacitor, the volume is $D_x D_y A_w$. Total all the components, and divide by 0.6. The aspect ration should be a minimum of 2 to a maximum of 5 for the length to end diagonal, but this is also a function of component size. For example, a $9 \times 3 \times 2$ may give the calculated needed volume and a good aspect ratio, but the wound inductors may be 3 inches in diameter. Either all the inductors will be aligned along the 9×3 inch direction or the height must change. This example may work, but quadtrature is violated and cross talk may be a problem.

对于连接器、圆形电容或任何圆形元件，体积均为 O_d 的平方乘以长度。对于压接使用的电容，体积为 $D_x D_y A_w$ 。然后将所有元件体积求和，并将结果除以 0.6。对于滤波器外形来讲，长度应对角线长度的 2~5 倍，对于元件这一准则同样有效。例如，一个 $9 \times 3 \times 2$ 的元件会具有较好的外形比，但是对于绕制的电感来讲如果直径是 3 英寸的话，那么要么将电感沿 9×3 英寸截面法向的方向排列，要么就要更改滤波器的高度。增加高度那么虽可以排布，但串扰会成为一个新的问题。

6. Design and build the case, or container, based on the components and volume just determined, and make sure that there are no solder or weld voids, which can allow radiation or destroy the potential of passing environmental tests, such as for humidity and salt spray. Have the case silver plated for better surface conduction. Also, aluminum is often used for better conduction, giving lower radiation. This is plated for even better conduction for lower radiation and for ease of soldering. This container will be silver plated by a military specification plater if the unit is for military uses.

6、按前面的元件和体积的计算值，设计和构造滤波器外壳，并保障没有导致辐射和阻碍通过环境实验（如湿热和盐雾实验）的没有焊接好的缝隙。对外壳镀银可以改善壳表面的导电性。同样，由于铝具有较好的导电性并能降低辐射所以常常被用来制作外壳。对于铝外壳同样可以使用导电性更好的导体来电镀以便于降低辐射并利于焊接。如果滤波器为军用，那么外壳需要按军标镀银。

7. Install the components, and test the filter in the open container. Tack the lid down only for easy alteration or adjustment.

7、安装元件并测试在开放壳体中的滤波器，为便于调整，先只将壳盖用螺钉简单连接。

8. Adjust the filter for the desired loss, if needed, by the following steps:

Add lossey components (Section 4.4).

Add small line-to-line capacitors (X capacitors) in parallel to the existing capacitors. Keep the lead length as short as possible.

Add ferrite beads if the current is low enough (typically 5A limit).

Add several turns on the inductors (watch for saturation). If this filter is a T, whatever turns added to the central inductors of the multiple T, increase the turns by half on the two outer inductors. They are half the value of the inner inductors.

Add an RCSHU (a resistor and capacitor in series across the line; see Section 5.7). Adjustments move the designer from either the ballpark property or the playing field to home plate with lossey components or line-to-line capacitors.

8、通过以下步骤将滤波器调整到所需的损耗值：

- 增加损耗元件（4.4 节）。
- 在已有的线间电容上并联小电容（X 电容），使电容管脚尽可能短。
- 如果电流足够低（典型以 5A 为限）时可以用加磁珠的方法。
- 增加电感匝数（注意饱和问题）。如果滤波器是多级 T 型，最外侧的两个电感增加的匝数是中心电感增加匝数的一半。
- 增加一个 RCSHU 电路单元（电阻和电容串联后并于线间，见 5.7 节）。通过使用线间电容或损耗元件，让设计者的调整设计从棒球场或运动场最终到达目的地。

9. Make sure that the end product is buildable and repeatable for production.

9、确认最终的滤波器产品是可生产和重复制造的。

§19.2 Filter in Tandem

§19.2 前后层叠连接的滤波器

This next section discusses a filter expanding from one section to two sections to three sections, and so on. This book states repeatedly (as when going from a single to a double L in Table 19.2) that as the section grow, the size of the components falls. The test problem is as follows:

本节讨论的是滤波器从单节向 2 节到 3 节等多级电路结构的扩展。本书此处重复论述了（同表 19.2 中从单节向双 L 型变化的情况相同）滤波器节数增加和元件参数下降的情况，例如如下问题：

Line frequency, 400Hz

Line voltage, 120V

Maximum line current, 6A

Needed loss, 60dB at 20kHz

This is solved first for the L then the T and followed by the π filter, only to prove that the same holds true for all three type (Tables 19.3, 19.4, and 19.5).

先求解 L 型滤波器的情况，接下来是 T 型和 π 型，当然此处只是为了证明对于三种滤波器类型其设计方法是相同的（表 19.3、19.4 和 19.5）。

Table 19.3 L filter Change as Sections Are Added

	F_0	L	C	Extension	
				L	C
1	405	7.860	19.6	7.860	19.6
2	2820	1.130	2.82	2.260	5.64
3	5170	0.615	1.54	1.85	4.62
4	6760	0.470	1.18	1.88	4.72
5	7760	0.410	1.02	2.05	5.10
6	8400	0.378	0.95	2.26	5.7

Table 19.4 T filter Change as Sections Are Added

	F_0	L	C	Extension	
				L	C
1	940	1.700	8.46	3.40	8.46
2	3130	0.508	2.54	2.032	5.08
3	5075	0.314	1.56	1.884	4.68
4	6460	0.246	1.23	1.968	4.92
5	7500	0.215	1.07	2.15	5.35
6	8035	0.198	0.99	2.37	5.94

Table 19.5 π Filter Changes as Sections Are Added

	F_0	L	C	Extension	
				L	C
1	555	5.735	7.16	5.735	14.32
2	2520	1.263	1.578	2.526	6.312
3	4730	0.672	0.841	2.016	5.046
4	6360	0.500	0.626	2.000	5.008
5	7450	0.427	0.534	2.135	5.340
6	8155	0.390	0.488	2.340	5.850

The program is the one used in Chapters 13 and 14. This is a low current, and

the maximum should be four sections but six are given. The value of L is in μH and C in μF . The first L and C are the individual component values, but the final value for L and C are the total component values for the filter. Note how the total L and C drop in value from one to three sections in Table 19.3, but little is gained past three sections. Little self-resonant frequency (SRF) is gained in moving the capacitor value from 1.54 (1.6 μF) to 1.181 (1.2 μF). The circuit can be balanced, with better SRF, moving the 620 μH to 310 μH . The T filter in Table 19.4 is the same as the L in Table 19.3. It is ridiculous to go beyond three sections. The 314 μH inductance is the value in each arm, or the total inductance for this one T is 628 μH . The central inductors are twice this initial value, or 628 μH each. Round these to even values, and the three-section T circuit is shown in Figure 19.2. The balanced circuit is shown in Figure 19.3.

此处计算软件使用的就是 13 章和 14 章使用的那个软件。这是一个低电流滤波器，最大应为 4 节，而表中列出了 1~6 节的情况。表中 L 值的单位是 μH ，电容的单位是 μF 。表中第一个电感和电容的值为单个元件的值，而最后的电感和电容的值为滤波器的该元件值的总和。注意表 19.3 中总的电感和电容的值是如何随电路从 1 到 3 节变化而下降的，但是从 3 节以后再增加节数就下降很小了。电容值从 1.54 (1.6 μF) 变化到 1.181 (1.2 μF)，但 SRF 却几乎没有太大变化。同样这个滤波器电路可以采用平衡电路设计，这样会有就较好的 SRF，同样电感也可由 620 μH 变为 310 μH 。表 19.4 中的 T 型滤波器也与表 19.3 中的 L 型滤波器情况相类似。可见，电路设计超过 3 节是比较荒谬的。T 型滤波器电感每边为 314 μH ，因此单 T 型滤波器的总电感为 628 μH 。多极 T 型滤波器中心的电感是这个初始值的二倍即每个 628 μH 。最后将这些电感近似到标准值，则 3 节 T 电路如图 19.2 所示。平衡电路如图 19.3 所示。

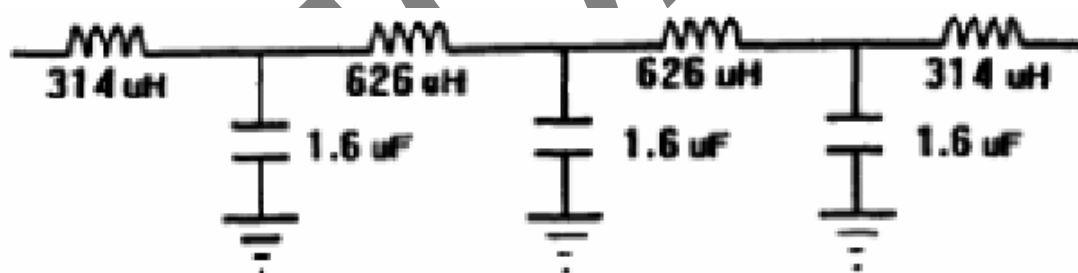


Figure 19.2 The multiple T.

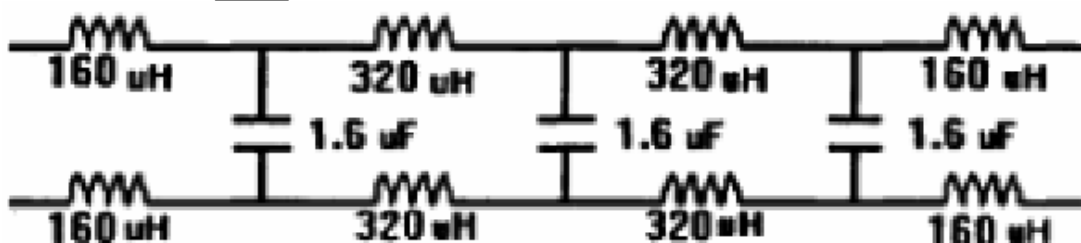


Figure 19.3 The balanced multiple T.

Note how the π filter values of the cutoff frequency F_0 is so much lower for the various sections in Table 19.5 compared with the T. Both the T and the π are

said to have 18dB loss per octave, but the T has this loss but is missing in the π . This is because of the low line impedance at 20kHz, estimated at 4Ω . If this had been equated with 220A specifications, the cutoff frequencies would have been similar to those for the T. Under these conditions, three sections may be too low, requiring a fourth section. This is caused by the value of F_0 . F_0 is cutting into the band pass, which is decided by the tenth harmonic of the power line frequency. The value listed for C is the value of the outside capacitors, and all inboard capacitors are twice this value. The four-section π is shown in Figure 19.4. In any of these applications, using 6dB headroom, the values are not critical. Round them to reasonable values. For the two end capacitors in the balanced π , I would use 0.6uF rather than 0.63uF.

注意在表 19.5 中，不同节数电路的 π 型滤波器与 T 型相比截止频率值是非常低的。按前面的说法 T 和 π 型滤波器的损耗为 18dB/倍频，但是实际上 T 型能达到此损耗而 π 型则不能。这是因为在 20kHz 频率下电源线具有低阻抗，约为 4Ω 。当然如果这个滤波器使用 220A 规范的条件来计算，那么 π 型的截止频率将与 T 型滤波器相同。在这些条件下，3 节的 π 型滤波器损耗或许太低了，因而需要 4 节电路。这是由于 F_0 的值的要求导致的，因为 F_0 的值切入等于 10 倍电源线频率所确定的导带频段。另外，此处列出的电容值是外部电容的值，内侧的电容值是此值的二倍。4 节 π 电路如图 19.4 所示。实际上计算得到的这些数值都不是典型值，所以需要将它们近似到合理的值。因而同时还需要考虑 6dB 的余量。如对于平衡 π 型电路两端的电容，我会使用 0.6uF 的电容而不是 0.63uF 的电容。

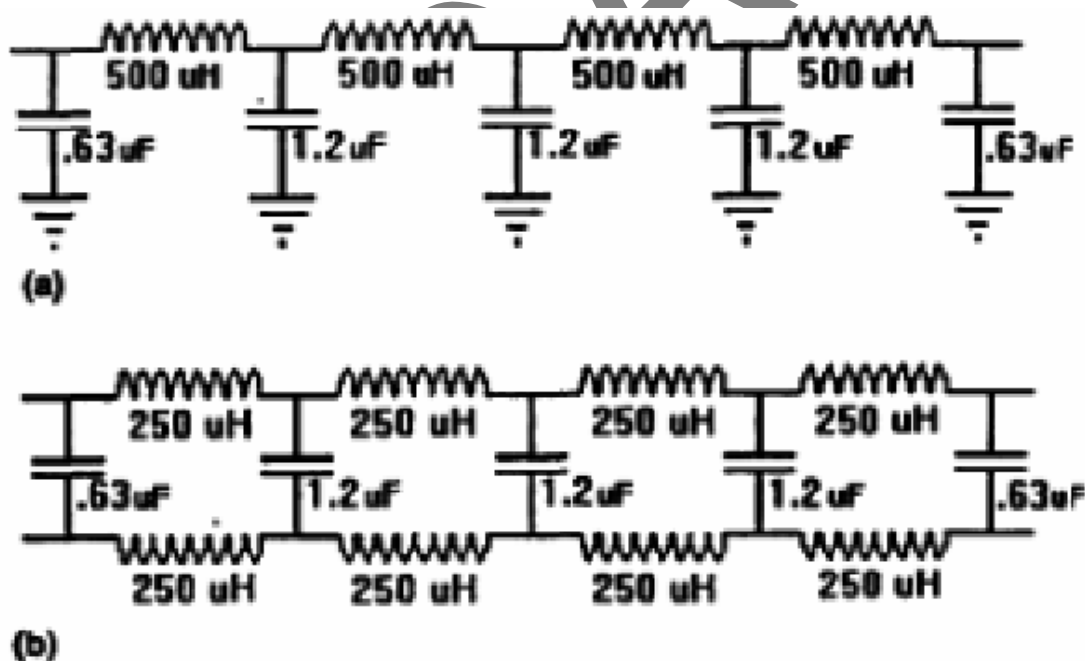


Figure 19.4 (a) Multiple π and the (b) balanced π .

Comparing the L, T and π sections, the total inductance and capacitance drop greatly from one section to two. A reasonable drop repeats going from two sections to three sections. A small drop occurs from three to four sections. This is followed by a modest increase from four to five sections and again from five sections to six. If the problem is being caused by a low SRF, adding a section

may help. Going to a balanced arrangement will almost double the inductor SRF, and this should help. Note here how the concern is for the SRF mainly for the inductor. This is because, unless the discussion is very high current filters, the typical value of inductor required compared with the capacitor has an order of magnitude of SRF lower than the capacitor. Looking again at the three types discussed, the π is the least reasonable and should be used only when a 220A test specification is called for. The reason this happens is that the front-end capacitor is out of the circuit at the low frequencies because of the low line impedance. This capacitor aids filtering when the line impedance rises to a reasonable value. An easy way to calculate this improvement in lower total inductance and capacitance is through the equations listed earlier. These are repeated here: they cannot be differentiated because they are not continuous functions.

对于 L、T 和 π 型电路，总的电感和电容值在电路从 1 节到 2 节变化时下降十分明显。但从 2 节到 3 节变化时下降就不剧烈，而从 3 节到 4 节变化时却下降很小。而在从 4 到 5 和 5 到 6 变化时却会有一定的增加。如果问题是由较低的 SRF 导致的，那么增加一节电路会有帮助，而且使用平衡电路设计会使 SRF 加倍，这也会有助于解决问题。注意，为何对于 SRF 问题主要关注电感值呢？这是因为除了大电流滤波器的情况，典型值的电感与电容相比其 SRF 比电容要低一个量级。再回顾一下讨论过的三种类型的滤波器， π 型是最不合理的而且应只用在 220A 测试规范要求的项目上。原因是，前后端的电容在低频率下因为较低的电源线阻抗而不起作用，直到电源线阻抗上升的一个合理的值，此电容才会起滤波作用。如果想计算总电感和电容值较低的电路的改善情况，则可以使用较早给出的等式来计算。在此处重新列出这些等式。这些等式不能微分，因为它们是不连续函数。

Loss required = dB
Loss per octave for filter = L
No. of octaves = X = dB/L

Frequency at needed loss = F
Cutoff frequency = F_0 = $F/2^X$

$$F_0 = \frac{F}{2^{\frac{L}{6}}}$$

As the value of L doubles and triples because of a higher number of filters in tandem, the denominator is reduced and the cutoff frequency rises. The loss L can be calculated from

因为较高的滤波器前后层叠数目，损耗值 L 会加倍或升高到三倍，此时，分母减小而截止频率上升。损耗 L 可由下式计算

$$L = \text{loss for } \pi \text{ or T} = (2N+1)6$$

$$L = \text{loss for an L} = 12N$$

The lower value of (loss) L is for the π and T filter; the upper value of (loss) L

is for the L filter (Table 19.6).

较低的损耗L是对应 π 型和T型滤波器的 较高的损耗L是对应L型滤波器的(见表 19.6)。

Table 19.6 Loss per Octave as Tandem Number Increases

Filter	Number of filters in tandem						
	1	2	3	4	5	6	7
L	12	24	36	48	60	72	84
π	18	30	42	54	66	78	90
T	18	30	42	54	66	78	90

§19.3 Q

§19.3 Q 值

The value of the circuit Q of the filter must be low, as stated (without explaining the reason) often in this book. If the Q is low enough, the number of resonant rises is 1 less than the filter sections. The resonant rise level is also a function of Q. The input voltage level of the resonant rise frequency times the Q of the circuit at that frequency equals the voltage output at this frequency. If high-quality capacitors are used, the Q of the circuit will fall to the inductors because capacitors normally carry a much higher Q rating, typically 10 times, than the inductors. For a single L circuit, the equation for Q is

如本书一直强调的(但没有解释原因), 滤波器电路的 Q 值一定要低。如果 Q 值足够低, 那么谐振增益点比滤波器节数少 1。谐振增益的程度同样也是 Q 值的函数。一般谐振增益频率下的输入电压乘以电路的 Q 值等于此频率下输出的电压。如果使用了高品质电容, 那么电路的 Q 值就会下降到电感的 Q 值, 这是因为电容的 Q 值往往很高, 通常是电感 Q 值的十倍。对于一个单 L 型电路, 其 Q 的表达式为

$$L = \frac{R_d}{2pF_0} \quad X_l = \frac{2pFR_d}{2pF_0} = \frac{FR_d}{F_0} = KR_d$$

$$Q = \frac{X_l}{R_d} = K$$

This value of Q is for one inductor. The value of the Q will be much lower than K because the design impedance R_d is lower than the operating impedance of the load. These simple equations do not figure in the dc resistance of the inductor, the line impedance, or the equivalent series resistance of the capacitors. This is another reason the design criterion sets the cutoff at least 10 times the line frequency and the headroom of 6dB. The line harmonic content should be low enough by the time the circuit Q is high enough to cause ringing or a resonant rise. In multiple circuits, the Q is a function of the total inductance. The value of

Q must be multiplied by the number of inductors, but as the cascaded sections increase, the value of F_0 rises, lowering the individual inductance, and also the total inductance (up to four) decreases. For T and π filters, the equation for the value of L in the loss equation is $6(2N+1)$ dB. For the L, the loss per octave is $12N$ dB. Either of these two values replaces the value of L in the previous section. The first equation is for either T or π and the last is for L. N is the number in tandem.

这个 Q 值表示的是一个电感的情况。此时这个 Q 值会远低于 K 值，这是因为设计阻抗 R_d 低于负载的工作阻抗。这个简单的公式没有考虑电感的交流阻抗、电源线阻抗和电容的等效串联阻抗等因素。这也是设计标准将截止频率设定在至少是电源线频率的 10 倍频的频率下和损耗预留 6dB 余量的另一个原因。在电路的 Q 值高到会导致谐振和振铃时，就需要电源线的谐波含量足够低。在多级电路中，Q 值是总电感的函数，此时 Q 值必须要乘以电感的数目，但是当层叠数增加时， F_0 值会升高，这又会降低了单个电感值，从而导致总电感（4 个以上）降低。对于 T 型和 π 型滤波器，损耗 L 的值为 $6(2N+1)$ dB。对于 L 型滤波器，损耗为 $12NdB/倍频$ 。这时要用这两个表达式代替前面章节中的式子。第一个用在 T 和 π 型电路上，后一个用在 L 型过滤器上。N 是前后层叠数目。

$$F_0 = \frac{F_i}{2^{\frac{dB}{(2N+1)6}}}$$

$$L = \frac{R_d}{2\pi F_0} = \frac{R_d 2^{\frac{dB}{(2N+1)6}}}{2\pi F_i}$$

$$X_i = \frac{2\pi F R_d dB / 2^{(2N+1)6}}{2\pi F_i} = \frac{F R_d 2^{\frac{dB}{(2N+1)6}}}{F_i}$$

$$Q = \frac{N X_i}{R_d} = \frac{F N 2^{\frac{dB}{(2N+1)6}}}{F_i}$$

The terms are restated here. The needed loss at the problem frequency (dB); the tandem number N, the problem frequency F_i , and the Q needed are known. Substitute 1 for Q, and solve for F. This is the approximate frequency, where Q is 1 (because of losses not accounted for, the actual value of F will be higher). Does this frequency fall near any power line harmonic, especially the odd harmonics, or near any known problem frequency? If yes, or just to be safe, add an RC shunt to this filter, where X_c will equal R_d at this frequency F. If another RC shunt is required for other reasons, only one is needed. Opt for the lower frequency RC shunt. If there are higher frequency Q problems, opt for a higher quality capacitor that will have a higher Q and higher SRF. Also, in this case, make sure that the resistor use in the RC shunt is noninductive in this case.

此处再次强调需要了解的各项：问题频率点下所需的损耗（dB）、滤波器层叠数目 N、问题

频率 F_r 和 Q 值。将 1 带入 Q ，并解出 F ，此 F 是 Q 值为 1（因为没有考虑损耗，实际的 F 值会高些）的近似频率。现在要考虑此频率与各次谐波尤其是奇次谐波或其它已知的问题频率点接近么？如果接近，或为安全起见，需要在此滤波器增加一个在频率 F 下 X_c 等于 R_d 的 RC 旁路。如果因为其它的原因需要另一个 RC 旁路（只需要一个）那么选择频率较低的 RC 旁路。如果有高频 Q 值问题，就需要选择具有高 Q 值和高 SRF 的高品质电容。同样在本例中，要确认 RC 旁路中使用的电阻是无感型的。

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